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MSC TECHNICAL REFERENCE DOCUMENT

INDEX

MSX HOME PERSONAL COMPUTER SYSTEM

HARDWARE SPECIFICATION

(RELEASE 3.1)

04/05/84

Hardware specification for MSX HOME PERSONAL COMPUTER SYSTEM

CONTENTS

Hardware specification for MSX HOME PERSONAL COMPUTER SYSTEM

*This document specifies the U.S./European version of MSX system.

CHAPTER 1

SUMMARY OF HARDWARE

SUMMARY OF HARDWARE

1.1 SPECIFICATION

1.1.1 Required Components

o	CPU	4 MHz Z-80A compatible
o	Memory	ROM 32K (MSX system software) RAM minimum 8K (16K* recommended)
o	Screen Display	Text display capability 40 x 24 (refer to section 2.4) Graphic 256 x 192 Color 16
o	Cassette tape	FSK format 1200/2400 Baud
o	Sound	8 Octave, 3 Voices
o	Character Set	Alphanumeric, Japanese, Graphic (Japanese version) Alphanumeric, European, Graphic (International version)
o	Keyboard	U.S./Europe, French*, German*, Japanese
o	Expansion Slot	Software cartridge, expansion BUS slots
o	Joystick	1 or 2*

1.1.2 Recommended Extensions for U.S./Europe

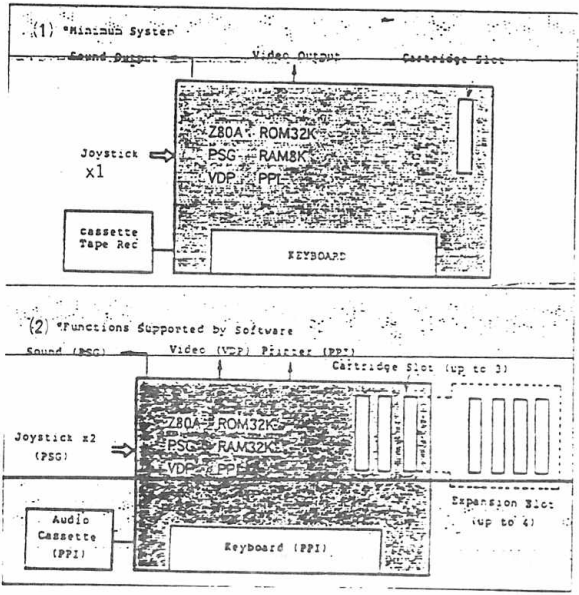
o	Memory	RAM 64K* total
o	Expansion Slot	Second
o	Video	RF output

1.1.3 Standardized Optional Extensions

o	Screen Display*	80-column text
o	Clock*	Battery backed-up CMOS
o	Communications*	RS-232
o	Floppy Disk*	According to each company. Format is MS-DOS compatible
o	Printer*	8 bit parallel

* Items with asterisk may not be build-in in the minimum system.

1.2 SYSTEM CONFIGURATION



CHAPTER 2

HARDWARE SPECIFICATION

HARDWARE SPECIFICATION

2.1 LSI

- o CPU — Z-80A Compatible
  CLOCK 3.579545MHz (NTSC Color sub carrier frequency)
  1 WAIT in M1 CYCLE
- o VDP — TI TMS-9918A Compatible
- o PSG — GI AY-3-8910 Compatible
- o PPI — Intel i-8255 Compatible

2.2 MEMORY

- o ROM — MSX BASIC 32KB
- o RAM — 8KB or more

NOTE

Basic unit has four logical slots, so the total memory space can be expanded up to 256KB. Each logical slot can be expanded to have up to 4 physical slots, total of 16 slots. So in this case, maximum memory space is 1 megabyte.

BASIC ROM occupies address 0 to 7FFF, RAM address starts from FFFF and grows downward on the memory map to 8000.

For details refer to 4.1 memory map.

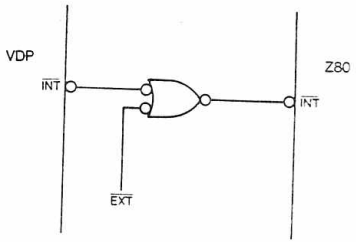
For U.S. Market we recommend 64K so the machine can easily be upgradable to MSX-DOS, although BASIC ROM will only use 32K RAM.

2.3 INTERRUPT

- MNI — Not used. MSX ROM only provides RAM hook.
- INT — Accept interrupts from VDP and cartridge. The interrupt is Z-80 mode 1. (Branch to 38H) MSX system software uses interrupt from VDP for timer count. The interval of the interrupt is 60Hz in NTSC and 50Hz in PAL/SECAM version.

NOTE

It is not possible to support NMI under MSX DOS environment because address 66H, which is the entry vector for NMI, is occupied by FCB data for DOS.



2.4 SCREEN DISPLAY

- o LSI — TI TMS9918A Compatible
- o Character set — Alphanumerical + European + Graphic
  256 patterns 6x8 dots
- o Color — 16 colors
- o Sprites — 32 sprites. Maximum 4 sprites on the same horizontal line.
- o List of display modes

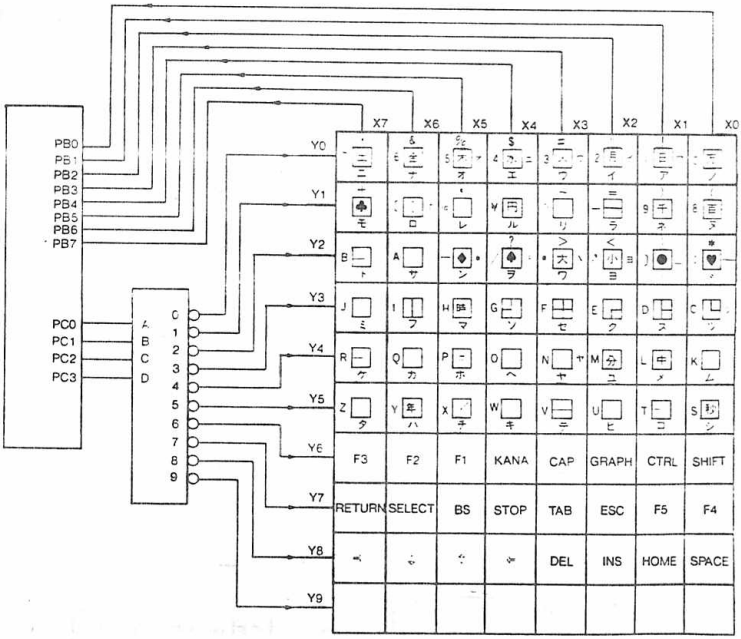
MODE		RES.	SIZE	NO.△	COLOR	SPRITE	NUMBER OF CHARACTERS
Graphic I	LSI Spec.	256 x 192	8 x 8	256	16 colors	YES	32 x 24
	Suggested value	240 x 192					29 x 24
Graphic II	LSI Spec.	256 x 192	8 x 8	768	16 colors	YES	32 x 24
	Suggested value	240 x 192					29 x 24
Multi-color	LSI Spec.	64x48blk	4 x 4 /block	-	16 colors	NO	32 x 24
	Suggested value	64x40blk					29 x 24
Text	LSI Spec.	256 x 192	6 x 8	256	2 colors out of 16 colors	YES	40 x 24
	Suggested value	240 x 192					39 x 24

Suggested value to use: the 8 pixels from left and right of horizontal are not used by software.

△ The number of patterns

2.5 KEYBOARD

- o Layout — Refer to figure
  - U.S./European
  - French
  - German
- o Scanning — Software scanning driven by VDP interrupt
- o Number of keys — 70 plus optional dead key
- o Matrix diagram



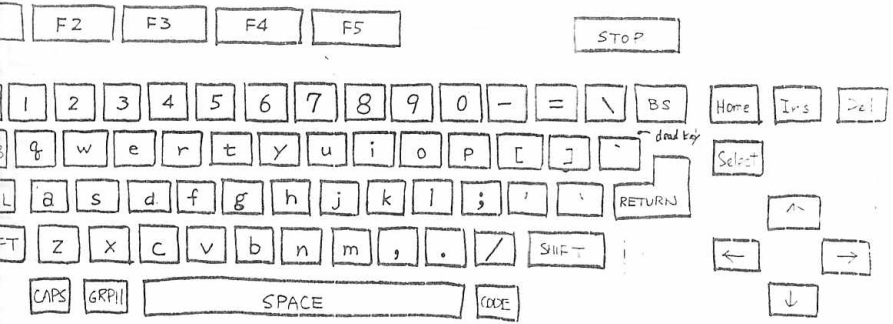
Y	X	0		1		2		3		4		5		6		7	
		char	code	char	code	char	code	char	code	char	code	char	code	char	code	char	code
0		0	30	/	31	2	32	3	33	4	34	5	35	6	36	7	37
	S	)	29	!	21	②	40	#	23	$	24	%	25	^	5E	&	26
	G	○	09	¼	AC	½	AB	¾	BA	∩	EF	‰	BD	⌐	F4	⌐	FB
	G S	◙	0A			²	FD	ⁿ	FC					J	FS		
	C	δ	EB	ƒ	9F	♯	D9	ς	BF	¢	9B	ÿ	98	∝	EO	β	E1
	CS	△	D8	¡	AD	₧	9E	¶	BE	£	9C	¥	9D	--			
1		8	38	9	39	—	2D	=	3D	⁄	5C	[	5B	]	5D	;	3B
	S	*	2A	(	28	‖	5F	+	2B	┤	7C	~	7B	}	7D	:	3A
	G	∞	EC	•	07	┼	17	±	F1	╱	1E	☺	01	♪	0D	♠	06
	G S			■	08	┼	1F	═	F0	┼	16	☻	02	♫	0E	♦	04
	C	ϒ	E7	ς	87	∈	EE	⊕	E9			∅	ED	ω	DA	¤	97
	CS	⌐	EZ	Ç	80							⊖	E8	Ω	EA	Ω	86
2		'	27	;	60	;	2C	.	2E	⁄	2F	:		¿	61	b	62
	S	=	22	~	7E	<	3C	>	3E	?	3F	≈	—	A	41	B	42
	G	♣	05	∿	BB	≤	F3	≥	F2	╲	1D	÷	dead key	■	C4	┼	11
	G S	♥	03	≈	F7	«	AE	»	AF	┼	F6	'		!	FE	-	
	C	¡	B9	°	E5	å	86	Ø	A6	○	A7	`		¨	84	λ	97
	CS	∏	B8	Σ	E4	Å	8F			¿	A8	^		¨	8E		
3		c	63	d	64	e	65	f	66	g	67	h	68	i	69	j	6A
		C	43	D	44	E	45	F	46	G	47	H	48	I	49	J	4A
	G	◇	BC	■	C7	◥	CD	┼	14	┼	15	▌	15	▐	DC	■	0B
	G S	•	FA	■	C1	▶	CE	■	D4	┼	10	■	D8	▐	DF	■	0A
	C	⁻	8D	¨	8B	↑	8C	ö	94	ü	81	¥	B	´	A1	ß	91
	CS					·		Ö	99	Ü	9A	Ã	B			Æ	92
4		K	6B	ℓ	6C	m	6D	n	6E	o	6F	p	70	q	71	r	72
		K	4B	L	4C	M	4D	N	4E	O	4F	P	50	Q	51	R	52
	G	▨	DD	■	C8	♂	0B	┴	1B	■	02		0B		0C	┬	13
	G S		DE	·	C9	♀	0C	■	C3		C3	■	C	◢	CB	┼	A9
	C	~	B3	~	B5	^	E6	ñ	A4	ó	A2	ú	A3	ê	83	ô	93
	CS	⁻	B2	Õ	B4			Ñ	A5			┬	E3	-			
5		s	73	t	74	u	75	v	76	w	77	x	78	y	79	z	7A
		S	53	T	54	U	55	V	56	W	57	X	58	Y	59	Z	5A
	G	▥	D2	┼	12	▐	CC	▙	1A	◣	CF	■	10	┼	19	◘	CF
	G S	◣	D1				C5	◣	C5	◣	DO		E9	┼	AA	°	F8
	C	ë	89	ù	96	ê	82	ò	95	ê	88	è	8A	á	AO	ā	85
	CS					Ê	90										

c Keyboard layout

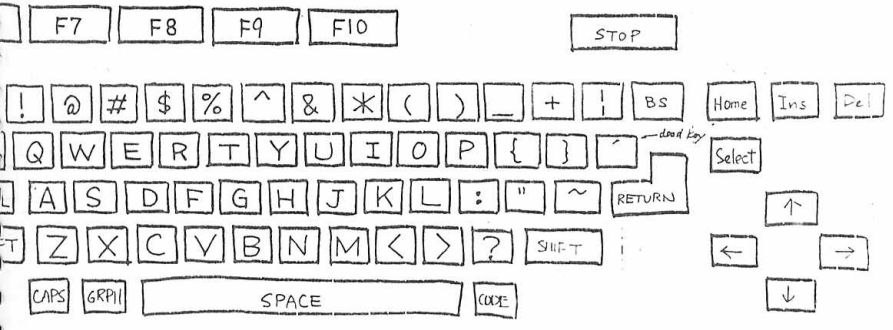
The following keyboard diagrams contain an optional dead-key. This dead-key is useful for European accented character input. For example, when one wishes to enter "â", one must first press the dead-key "^" and then press "a".

The dead-key will not be useful in the U.S. or U.K. Nor will it be useful in France and Germany, where specific French and German keyboards have been designed which include different dead-keys. Therefore this general dead-key should only be included on machines which will be marketed into minor European countries.

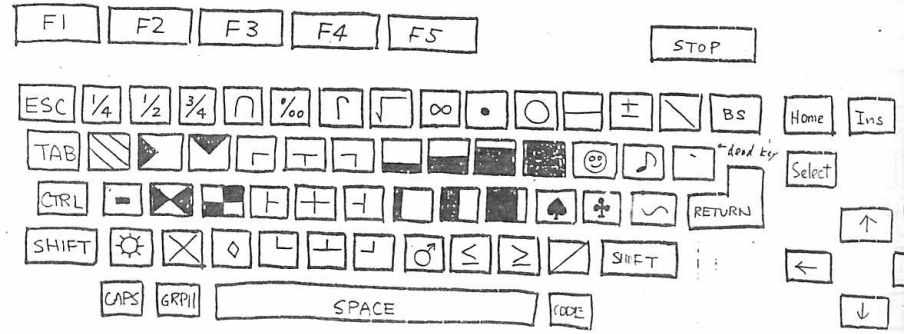
The keyboard diagrams show the dead-key to the left of the carraige return key, but this is probably not a good place for it, because it pushes the carraige return key too far to the right. Manufacturers may place this key where they wish.



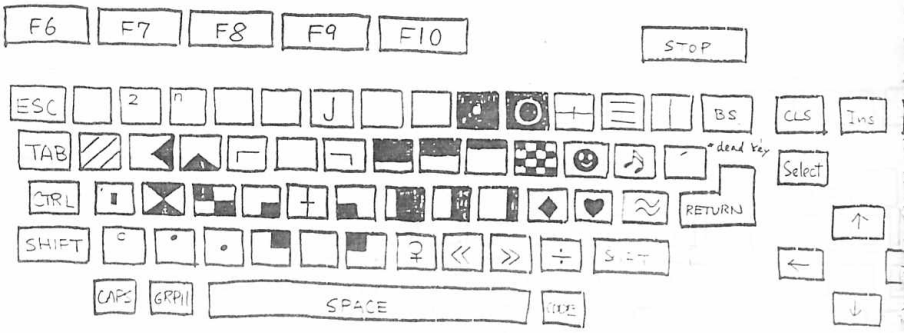
without Shift
without Graph
without code



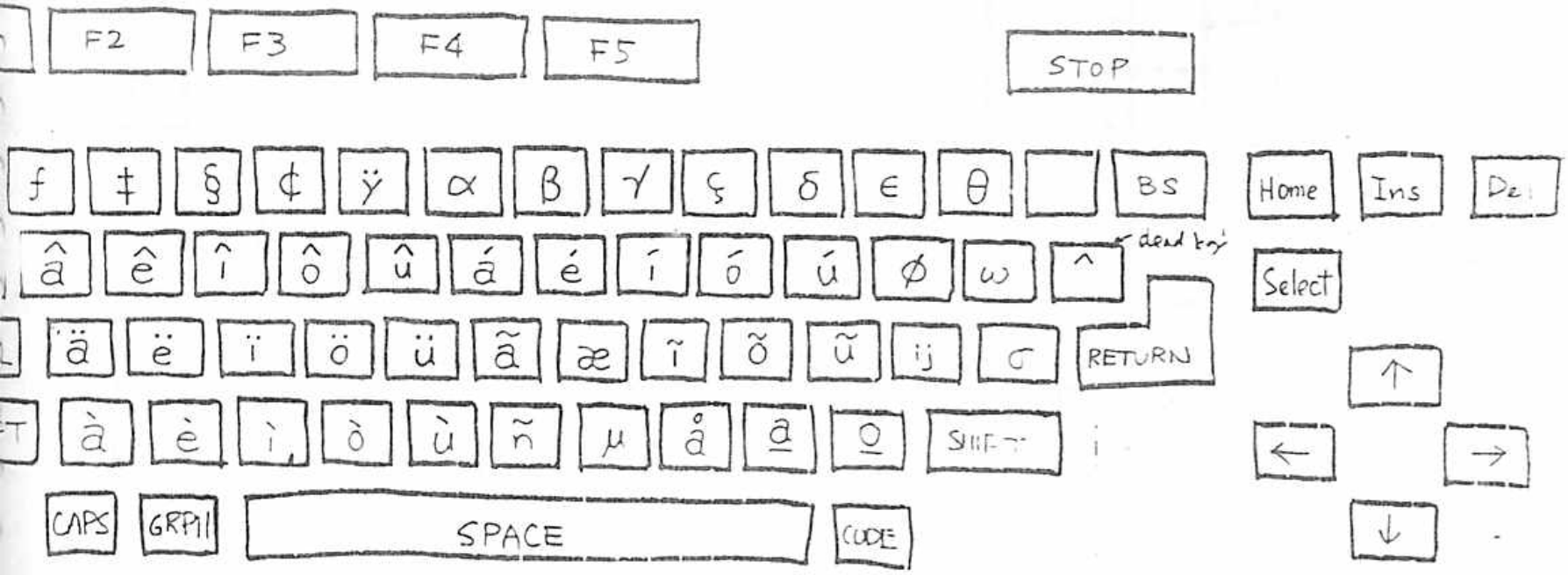
with Shift
without Graph
without Code



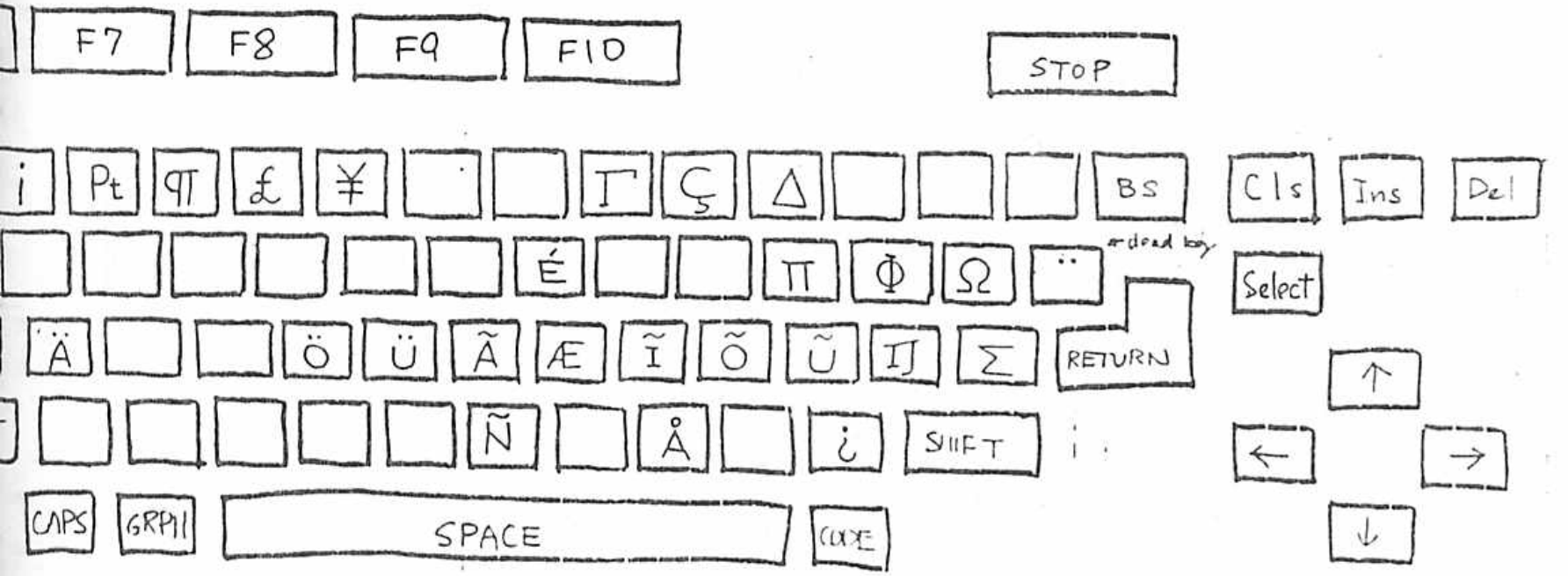
without Shift
with Graph
without Code



with Shift
with Graph
without Code



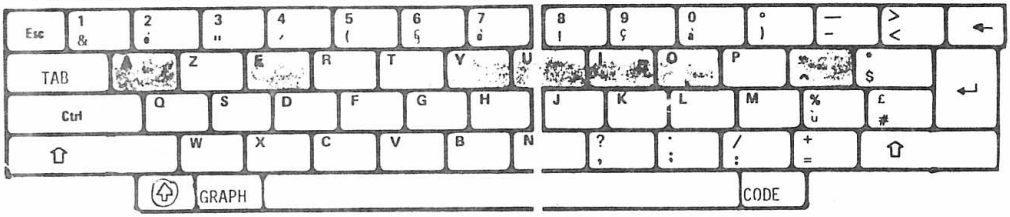
without shift
without Graph
with code



with shift
without Graph
with code

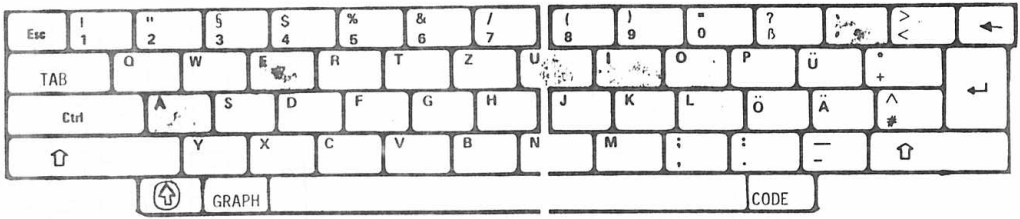
MSX French Keyboard

Caps Lock shifts numeric keys and)/° key. Dead keys are shaded.
Manufacturer may move less than/greater than key to lower left but must do so in keyboard hardware.



MSX German Keyboard

Caps Lock shifts A, O, and U umlaut keys. Dead keys are shaded.
Manufacturer may move less than/greater than key to lower left but must do so in keyboard hardware.



BASIC SPECIFICATION

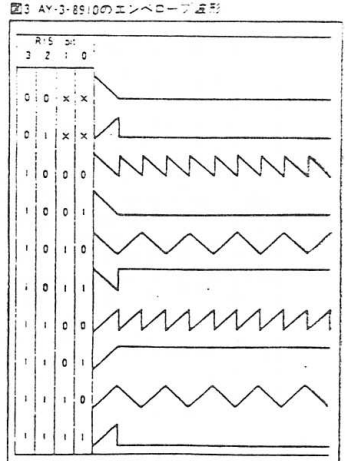
2.6 SOUND

- o LSI GI AY-3-8910 Compatible
- o OCTAVE 8 Octaves (3 Voices output)
- o SOUND EFFECT Yes
- o SOFTWARE SOUND OUTPUT 1 bit from output port
- o OUTPUT LEVEL -5dbm (If the system has output connector)
- o CONNECTOR RCA 2 pins (If the system has audio output connector)

REGISTER / BIT	B7	B6	B5	B4	B3	B2	B1	B0
R0	8-BIT Fine Tune A							
R1 Channel A Tone Period	4-BIT Coarse Tune A							
R2	8-BIT Fine Tune B							
R3 Channel B Tone Period	4-BIT Coarse Tune B							
R4	8-BIT Fine Tune C							
R5 Channel C Tone Period	4-BIT Coarse Tune C							
R6 Noise Period	5-BIT Period Control							
R7 Enable	I/O ENT		Noise			Tone		
	IOB	IOA	C	B	A	C	B	A
R8 Channel A Amplitude				M	L3	L2	L1	L0
R9 Channel A Amplitude				M	L3	L2	L1	L0
R10 Channel A Amplitude				M	L3	L2	L1	L0
R11 Envelope Period	8-BIT Fine Tune E							
R12	8-BIT Coarse Tune E							
R13 Envelope Shape Cycle					CONT	ATT	ALT	HOLD
R14 I/O Port A Data Store	8-BIT PARALLEL I/O on Port A							
R15 I/O Port B Data Store	8-BIT PARALLEL I/O on Port B							

図2 AY-3-8910のレジスタ構成

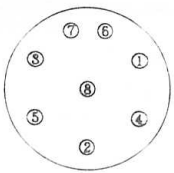
図3 AY-3-8910のエンベロープ波形



2.7 CASSETTE INTERFACE

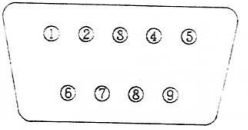
- o INPUT — From the earphone terminal of tape recorder
- o OUTPUT — To the microphone terminal of tape recorder
- o SYNCHRONIZATION — Asynchronous by the software
- o BAUD RATE — 1200 Baud (1200Hz - 1 wave "0", 2400Hz - 2 waves "1") (Default)

  2400 Baud (2400Hz - 1 wave "0", 4800Hz - 2 waves "1") Change by software (Tape recorder may have to be specified by the manufacturer when used under 2400 Baud mode)
- o MODULATION — FSK (Frequency Shift Keying) by the software
- o DEMODULATION — By the software. The system software automatically detects the baud rate when receiving the data.
- o MOTOR CONTROL — Yes
- o CONNECTOR — DIN 45326 (8 pin)
- o TABLE OF SIGNAL PINS

PIN NO.	SIGNAL NAME	DIRECTION	PIN CONNECTION
1	GND	---	
2	GND	---	
3	GND	---	
4	CMTOUT	OUTPUT	
5	CMTIN	INPUT	
6	REMOTE +	OUTPUT	
7	REMOTE -	OUTPUT	
8	GND	---	

2.8 INPUT/OUTPUT (JOYSTICK) PORT (1 OR 2* PORTS)

- o LSI — AY-3-8910 compatible
- o I/O — Input 4 bit, output 1 bit, bidirectional 2 bit per each port
- o LOGIC — Active high
- o LEVEL — TTL
- o CONNECTOR — AMP 9 pin compatible
- o LIST OF PINS

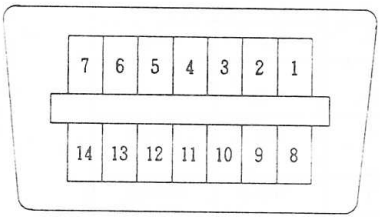
PIN NO.	SIGNAL NAME	DIRECTION	PIN CONNECTION
1	FWD	INPUT	
2	BACK	INPUT	
3	LEFT	INPUT	
4	RIGHT	INPUT	
5	+ 5V Δ	---	
6	TRG 1	INPUT/ OUTPUT	
7	TRG 2	OUTPUT	
8	OUTPUT	OUTPUT	
9	GND	---	

Δ Current capacity is 50mA each

2.9 *PRINTER INTERFACE

- o SPECIFICATION 8 bit parallel Handshakes by BUSY and STROBE signal
- o LEVEL TTL
- o CHARACTER CODE SAME AS MSX DISPLAY CODE
- o CONNECTOR AMP 14 pin compatible
- o LIST OF PINS

PIN NO.	SIGNAL NAME	PIN CONNECTION
1	PSTB	
2	PDB0	
3	PDB1	
4	PDB2	
5	PDB3	
6	PDB4	
7	PDB5	
8	PDB6	
9	PDB7	
10	N.C.	
11	BUSY	
12	N.C.	
13	N.C.	
14	GND	



2.10 FLOPPY DISK INTERFACE

- Contains 16K bytes of ROM at 4000H that includes:
  - * MSX-DOS KERNEL
  - * MSX DISK BASIC
  - * PHYSICAL DISK I/O DRIVER (Supplied by each manufacturer)

- The hardware interface is not specified. The physical disk I/O driver supplied by manufacturer should virtualize hardware differences.

- It is desirable to have a mechanism in the disk drive to detect whether the drive door has been opened. It reduces disk accesses which check for disk changes.

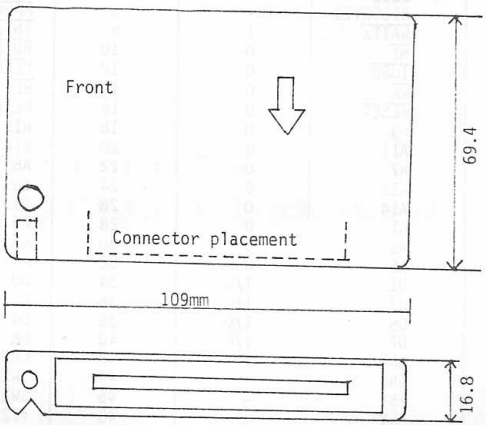
- Floppy formats are MS-DOS compatible

8 inch	SD	128 byte/sector
8 inch	DD	1024 byte/sector
5-1/4 inch	DD	512 byte/sector
3.5 inch	2DD	512 byte/sector (exactly same as 5-1/4" 96TPI
3 inch	2DD	512 byte/sector (exactly same as 5-1/4" 48TPI

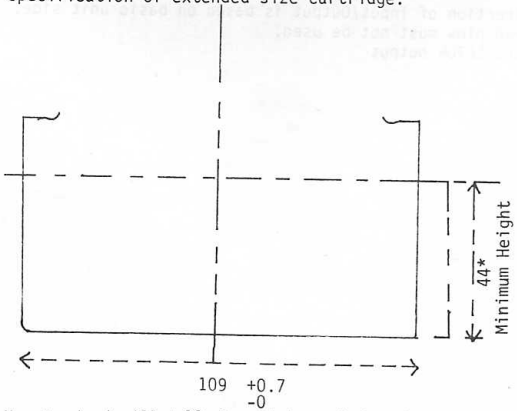
CHAPTER 3

CARTRIDGE

The internal specification of standard size cartridge
(all measurements in mm)



Specification of extended size cartridge.



* No standard will be enforced beyond the above minimum height

3.2 CARTRIDGE BUS

o LIST OF SIGNAL PINS

PIN NO.	NAME	I/O *	PIN NO.	NAME	I/O *
1	$\overline{CS1}$	O	2	$\overline{CS2}$	O
3	$\overline{CS12}$	O	4	$\overline{SLTSL}$	O
5	RESERVED	-	6	$\overline{RFSH}$	O
7	$\overline{WAIT}$Δ	I	8	$\overline{INT}$Δ	I
9	$\overline{M1}$	O	10	$\overline{BUSDIR}$	I
11	$\overline{IORQ}$	O	12	$\overline{MERQ}$	O
13	$\overline{WR}$	O	14	$\overline{RD}$	O
15	$\overline{RESET}$	O	16	RESERVED	-
17	A9	O	18	A15	O
19	A11	O	20	A10	O
21	A7	O	22	A6	O
23	A12	O	24	A8	O
25	A14	O	26	A13	O
27	A1	O	28	A0	O
29	A3	O	30	A2	O
31	A5	O	32	A4	O
33	D1	I/O	34	D0	I/O
35	D3	I/O	36	D2	I/O
37	D5	I/O	38	D4	I/O
39	D7	I/O	40	D6	I/O
41	GND	-	42	CLOCK	O
43	GND	-	44	SW1	-
45	+5V	-	46	SW2	-
47	+5V	-	48	+12V	-
49	SOUNDIN	I	50	-12V	-

* The direction of Input/Output is based on basic unit side.
Reserved pins must not be used.

Δ OPEN COLLECTOR output

o SIGNAL PIN ILLUSTRATION (Under lined signals are negative logic)

PIN NO.	NAME	DESCRIPTION
1	$\overline{\text{CS1}}$ Δ	ROM 4000~7FFF selected signal
2	$\overline{\text{CS2}}$ Δ	ROM 8000~FFFF selected signal
3	$\overline{\text{CS12}}$ Δ	ROM 4000~BFFF selected signal (for 256K ROM)
4	$\overline{\text{SLTSL}}$	Slot select signal
5	RESERVED	For future use only. Do not use this pin.
6	$\overline{\text{RFSH}}$	Refresh signal
7	$\overline{\text{WAIT}}$	Wait signal to CPU
8	$\overline{\text{INT}}$	Interrupt request signal
9	$\overline{\text{M1}}$	Fetch cycle signal of CPU
10	$\overline{\text{BUSDIR}}$	This signal controls the direction of external data bus buffer when the cartridge is selected. It is low level when data is sent by the cartridge.
11	$\overline{\text{IORQ}}$	I/O request signal
12	$\overline{\text{MERQ}}$	Memory request signal
13	$\overline{\text{WR}}$	Write signal
14	$\overline{\text{RD}}$	Read signal
15	$\overline{\text{RESET}}$	System reset signal
16	RESERVED	For future use only. Do not use this pin.
17~32	A0~A15	Address bus
33~40	D0~D7	Data bus
41	GND	Ground
42	CLOCK	CPU clock 3.579 MHz
43	GND	Ground
44, 46	SW1, SW2	Insert/remove detection for protection
45, 47	+5V	+5V power supply
48	+12V	+12V power supply
49	SOUNDIN	Sound input (-5dbm)
50	-12V	-12V power supply

NOTE

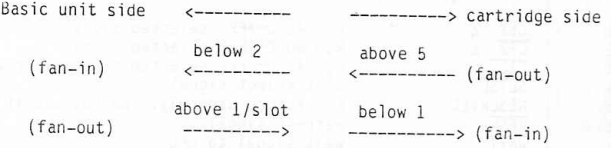
CS signals imply memory request and read signal. Therefore they cannot be used chip select for writable devices such as RAMs.

CARTRIDGE

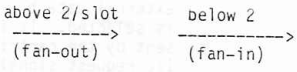
3.3 CONDITION OF CARTRIDGE CONNECTION

o Fan-in, Fan-out, (LS-TTL load)

Data and Address bus



o Control Signals



o Voltage level TTL level

CARTRIDGE

3.4 POWER CAPACITY

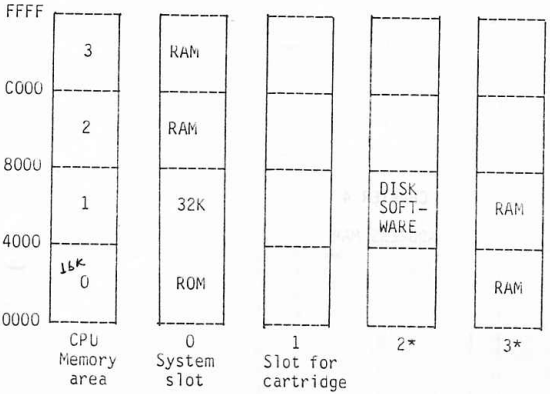
+5V	300mA/slot
+12V	50mA
-12V	50mA

CHAPTER 4

ADDRESS MAP

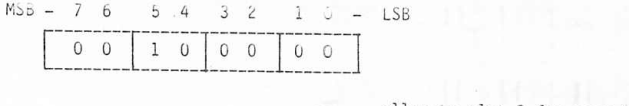
4.1 MEMORY MAP

- Following is an example of memory map.



- MSX BASIC uses the largest available contiguous RAM area that is installed from FFFF to 8000 for its system working RAM area. This can be placed in any slots including expansion slots.

- Slot select register, which is port A of 8255, maps thephysical memory space to the logical CPU memory space in 16K byte units (pages). For example, the following value in the slot select register allocates pages 0 and 1 from slot 0, page 2 from slot 2 and page 3 from slot 0.



Physical memory is always allocated to the same memory page in the CPU address space. It is not possible to allocate to a different page, like page 3 of slot 3, to page 0 of CPU memory space.

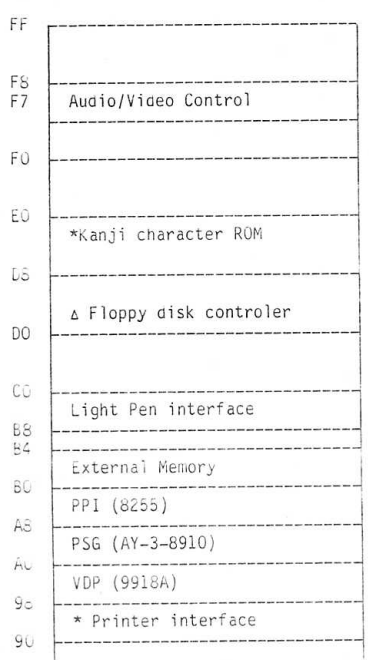
- Minimum system must have two slots, one for system, the other for cartridge.

NOTE

The word "slot" does not imply that it must have a connector for cartridges, however, a slot for cartridges must have a connector, of course. Refer to APPENDIX C.

- MSX-DOS requires 64K RAM

4.2 I/O ADDRESS MAP



4.3 I/O DEVICE DESCRIPTION

4.3.1 RS-232C

4.3.1.1 LSI Components -

i-8251 Communication interface chip
i-8253 Programmable interval timer chip

4.3.1.2 Port Address -

80H	R/W	8251 data port
81H	R/W	8251 command/status port
82H	R	Baud rate setting switches
83H	R	Configuration setting switches
83H	W	Interrupt mask register
84H	R/W	8253 counter 0
85H	R/W	8253 counter 1
86H	R/W	8253 counter 2
87H	W	8253 mode register

4.3.1.3 The Usage of Switch Port at Address 82H And 83H -

82H read - baud rate select

bit 0 - 3 : baud rate for receiver
bit 4 - 7 : baud rate for transmitter

value	baud rate
0	50
1	75
2	110
3	150
4	300
5	600
6	1200
7	2400
8	4800
9	9600
A	19200
B	N.A.
C	N.A.
D	N.A.
E	N.A.
F	disable*

*When value F is set as a baud rate, that function is disabled by software.

83H read - Set various functions

bit 0 - CD (carrier detect)*	
1 - auto line feed on receive**	1 - auto line feed
2 - Full/Half duplex	1 - Full duplex
3 - XON/OFF control	1 - Enable control
4 - Word length	1 - 8bits, 0 - 7 bits
5 - Parity Even/Odd	1 - Even
6 - Parity enable	1 - Enable
7 - Stop bit length	1 - 2 bits, 0 - 1 bit

* CD is a signal directly connected to carrier detect (pin 8) on the DB-25 connector.
** Add line feed on receiving carriage return.

NOTE

Bit 0 of the switch pulls up the CTS line of the 8251 (or [actually] it pulls down since CTS on 8251 is negative logic) to make it possible to send data even when CTS is not supplied from outside.

83H write - Set interrupt mask for receive

bit 0 - mask interrupt for receive 1 - mask interrupt
The initial value of this mask is 1 (disable interrupt).

4.3.1.4 Usage of 8253 Timer-counter To Generate Baud Rate - clock for 8251

- Frequency of crystal
  The frequency of the crystal:
  1.2288 MHz

- Usage of counter channel
  CH0 - Rx baud rate clock
  CH1 - Tx baud rate clock
  CH2 - General interrupt timer .. connect to IRQ

4.3.2 PRINTER PORT

4.3.2.1 Port Address -

90H	R	Busy status : bit 1
90H	W	Strobe output : bit 0
91H	W	Print data

4.3.3 VDP PORT

98H	R/W	Video Ram data
99H	R/W	Command and status register

4.3.4 PSG PORT

A0H	W	Address latch
A1H	W	Data write
A2H	R	Data read

4.3.5 PPI PORT

A8H	R/W	Port A
A9H	R/W	Port B
AAH	R/W	Port C
ABH	R/W	Mode registerr

4.3.6 External Memory (Sony)

B0H through B3H

4.3.7 Light Pen (Sanyo)

B8H through BBH

4.3.8 Audio/Visual Control

F7H	W	BIT4 - AV CONTROL	L - TV
	W	BIT5 - Ym CONTROL	L - TV
	W	BIT6 - Ys CONTROL	L - Super
	W	BIT7 - Video select	L - TV

4.4 NOTES ON I/O ADDRESS ASSIGNMENT

- I/O address 80-FF are assigned for system usage. The empty areas are reserved for system use.
  Although these addresses are defined here, software should not access those devices directly through the addresses listed above. Every access to the I/O must be done through the BIOS calls. This is to keep software independent from hardware differences. Manufacturers may change some hardware from the standard MSX system and is still able to maintain software compatibility by

supporting the hardware differences within the BIOS, so that the difference can be transparent to software.
The only exception is access to the VDP. Locations 6 and 7 of the MSX system ROM contain read and write addresses of VDP register. The software needing to access VDP very quickly may access VDP directly through those addreses stored in ROM.

o 00~7F are free addresses, however when different devices use the same address, they may not be accessed at the same time. Basically, special I/O devices not defined here should be placed in the memory space as memory mapped I/O. Refer to Appendix B.3.

Δ FDC may be placed in I/O space, but it must have a mechanism to disable it and only at the moment when the system accesses the FDC, is it enabled. This makes it possible to have more than one FDC interface in the system to handle different kinds of media.

4.5 8255 (PPI) BIT ASSIGNMENT

PORT	BIT	I/O	SIGNAL NAME	DESCRIPTION
A	0 1	OUTPUT	CS0L CS0H	0000~3FFF address slot select signal
	2 3		CS1L CS1H	4000~7FFF address slot select signal
	4 5		CS2L CS2H	8000~BFFF address slot select signal
	6 7		CS3L CS3H	C000~FFFF address slot select signal
B	0 thru 7	INPUT		Keyboard return signal
C	0 1 2 3	OUTPUT	KB0 KB1 KB2 KB3	Keyboard scan signal
	4		CASON	Cassette control signal (L-ON)
	5		CASW	Cassette write signal
	6		CAPS	CAPS lamp signal ("L" --> ON)
	7		SOUND	Sound input by software

4.6 PSG BIT ASSIGNMENT

PORT	BIT	I/O	CONNECTOR PIN NO.		NOTE
A	0		J3-PIN 1	1	FWD1
		I	J4-PIN 1 *	2	FWD2
	1		J3-PIN 2	1	BACK1
		N	J4-PIN 2 *	2	BACK2
	2		J3-PIN 3	1	LEFT1
		P	J4-PIN 3 *	2	LEFT2
	3		J3-PIN 4	1	RIGHT1
		U	J4-PIN 4 *	2	RIGHT2
	4		J3-PIN 6	1	TRGA1
		T	J4-PIN 6 *	2	TRGA2
	5		J3-PIN 7	1	TRGB1
			J4-PIN 7 *	2	TRGB2
	6		KEY LAYOUT Select 4		Japanese version only
	7		CSAR (CASSETE TAPE READ)		
B	0		J3-PIN 6	3	-- "H" LEVEL
	1	O	J3-PIN 7 *	3	-- "H" LEVEL
	2	U	J4-PIN 6	3	-- "H" LEVEL
	3	T	J4-PIN 7 *	3	-- "H" LEVEL
	4	P	J3-PIN 8		
	5	U	J4-PIN 8 *		
	6	T	PORT A INPUT SELECT		Selects J3/J4
	7		KLAMP (KANA LAMP L- ON)		Japanese version only

1 Available when bit 6 of port B is low used by JOYSTICK1
2 Available when bit 6 of port B is high used by JOYSTICK2
3 Turn to "H" level when use those pins as an input port.
  Tied an open collector buffer to the output. (Refer to Appendix C-1)
4 JIS layout - "H" level, syllable layout - "L" level

<Remark> PIN5 +5V
PIN9 GND

o On the minimum system, there is no J4 connector.

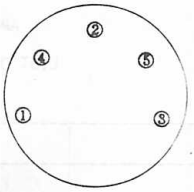
APPENDIX A

LIST OF CONNECTORS

PIN NAME	SPECIFICATION
1. Video output and composite video	DIN 5 PIN CONNECTOR Δ or RCA 2 PIN CONNECTOR
2. RF modulated signal	RCA 2 PIN CONNECTOR
CASSETTE	DIN 8 PIN CONNECTOR (DIN-45326)
I/O PORT	AMP 9 PIN CONNECTOR
PRINTER	AMPHENOL 14 PIN CONNECTOR
CARTRIDGE BUS	0.10 INCH (2.54mm) SPACE, 50 PIN CONNECTOR
AUDIO	RCA 2 PIN CONNECTOR

LIST OF CONNECTORS

△ DIN 5 PIN CONNECTOR SIGNAL PIN ASSIGNMENT

PIN NO.	NAME	PIN CONNECTION
1	+5V	
2	GND	
3	AUDIO	
4	MONITOR	
5	RF VIDEO	

APPENDIX B

NOTES ON SYSTEM EXPANSION

B.1 RAM EXPANSION

- The MSX BASIC needs contiguous RAM space starting from FFFF down to 8000. Therefore, additional RAM should be added to existing RAM to form contiguous RAM space.

- If the basic model has only 8K bytes of RAM, it is not possible to add RAM in the slot other than the original 8K in place, because the slot select logic treats memory space in 16K byte units. So an expansion cartridge that has 16K bytes adds only 8K bytes when it is placed at location C000 to FFFF. It is not possible to expand the RAM area by placing it at location 8000 to BFFF because there would be no RAM from C000 to DFFF. So cartridges for 16 KB basic systems, off the shelf, cannot be used on this 8 KB RAM system. Therefore it is important to make this point clear to the user. We don't recommend building a system which has only 8K bytes.

- The BASIC MSX software only uses RAM from 8000 to FFFF, so the RAM installed from 0 to 7FFF cannot be used by it.

B.2 SLOT EXPANSION

- To expand slots, the additional slots are expanded from a primary slot. Primary slots are those slots which are managed by the basic slot select register placed in port A of 8255. Therefore, to select the expanded slot, first select the primary slot to which the expanded slot is connected, and select the desired expansion slot.

- The location of the slot select register for the expanded slots is at memory address FFFF of the primary slot. To make it possible to differentiate this register from ordinary RAM, complement the output of the register. That is, when reading the register, the read data is the complement of the actual value of the register.

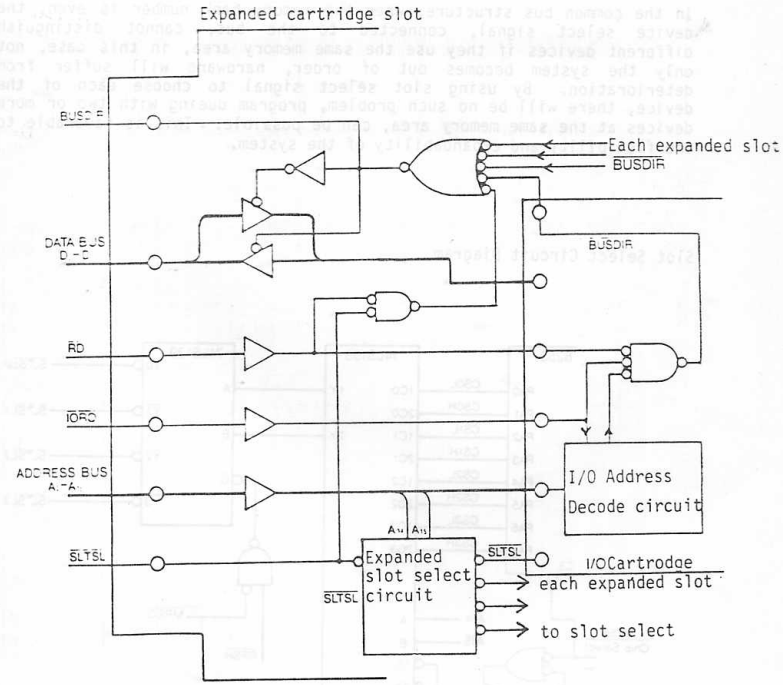
- The maximum number of cartridges that can be connected to the cartridge

bus is four. Therefore, buffers are necessary to put more than five slots to the system. The control signal that controls the direction of those buffers is BUSDIR. Those devices which send signals to the CPU and are placed in an expanded slot have to send BUSDIR signal as well the change the direction of the buffer from expanded slots to CPU. However, for the accesses to memory, it is possible to know the direction of the bus using the slot select signal to the primary slot, memory request signal and read/write signal. So the direction of the buffer should be controlled around the buffer circuitry. So, those cartridges which contain only ROM/RAM do not have to manage BUSDIR signal, so that make the cost of them cheap. But those cartridges that contain some devices which send signals to the CPU, that is, those devices that respond to INP instruction or those devices that is responsible to supply the address in response to the mode 2 of interrupt must force BUSDIR at 'L' level when they send data to CPU.

B.3 I/O EXPANSION

- In Z-80 based system, it is common to place I/O devices in I/O address space. But the MSX system design is so flexible and expandable, it is possible to add some I/O devices with cartridge that share same address space. If this is the case, none of those devices can be accessed properly.
  To avoid this situation, it is preferred to place I/O devices in the memory spaces because they are managed by slot select logic and no memory can be accessed simultaneously when they are placed in different slots. But the devices that placed in memory space cannot be accessed by the softwares that run in different slots. So those devices that are general to any software such as VDP have to be placed in I/O address space. Also in some case, it is cheaper to use I/O address space because only 8 bits address information should be decoded. We defined I/O address space from 80 to FF for those system devices. But the addresses below 7F are left free. Anybody may use this address space, but nobody can tell you that somebody uses same address that you are using. So we recommend to use memory address spaces rather than I/O address space. We will assign the reserved address to those devices that is thought as MSX standard device.

B.4 SAMPLE CIRCUIT OF EXPANDED SLOT



B.5 SLOT

- CONCEPT OF SLOT

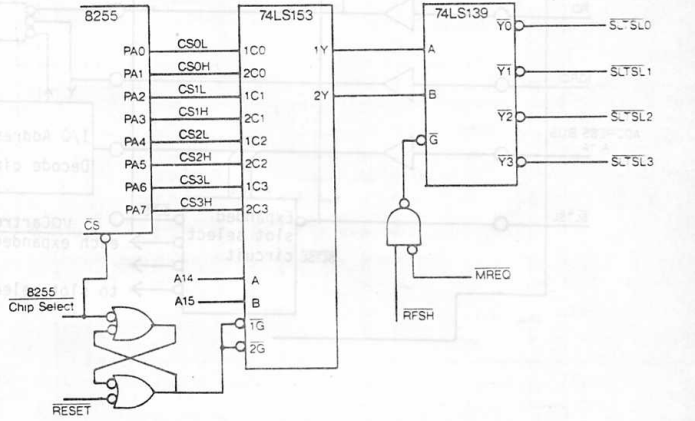
For a structure of 64 KB memory space, the concept of slot and memory bank is nearly the same. But CPU can choose the cartridge by the slot number in which it is inserted.

The slot concept is originated from the standpoint of the software, and so, the software is independent to the number of slot that has actual slot opening.

- ADVANTAGE OF SLOT STRUCTURE

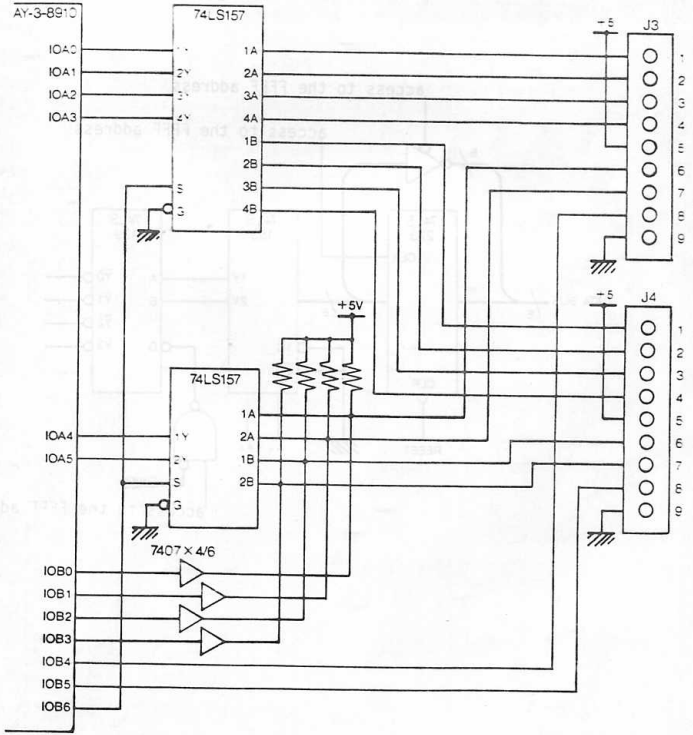
In the common bus structure, when the memory bank number is even, the device select signal, connected to the bus, cannot distinguish different devices if they use the same memory area, in this case, not only the system becomes out of order, hardware will suffer from deterioration. By using slot select signal to choose each of the device, there will be no such problem, program dueing with two or more devices at the same memory area, can be possible. This is favorable to the flexibility and expandability of the system.

Slot Select Circuit Diagram



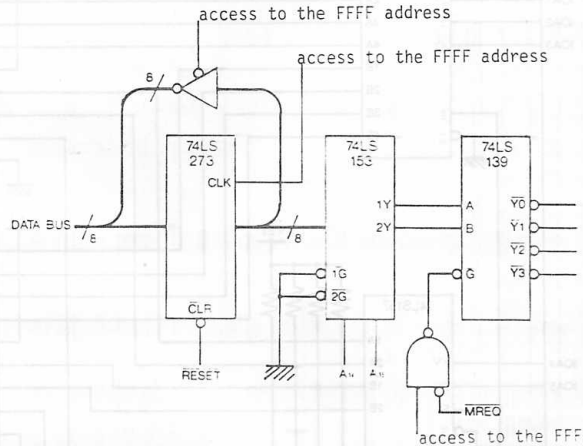
APPENDIX C

SAMPLE CIRCUIT DIAGRAM OF GENERAL I/O PORT



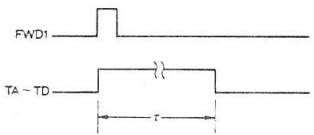
APPENDIX D

SAMPLE CIRCUIT DIAGRAM OF EXPANDED SLOT SELECT SIGNAL GENERATE LOGIC



APPENDIX E

GAME PADDLE TIMING DIAGRAM



τ=10μs to 3ms