ORIGINAL VERSION

SERVICE MANUAL
ORIGINAL

PERSONAL COMPUTER

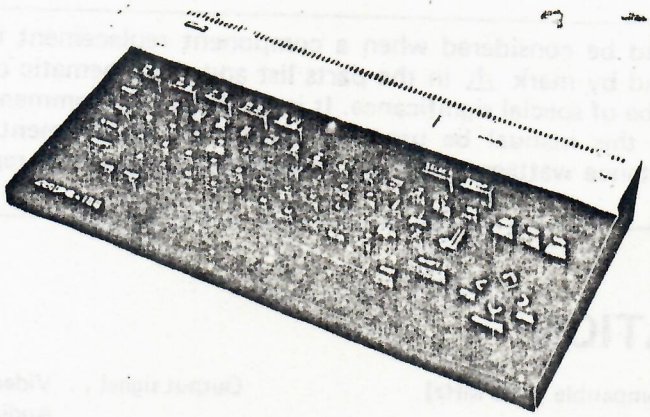
Chassis number is printed in the rating plate affixed to the bottom of the cabinet.

SANYO

Model MPC-100 (EU)

SERVICE REF. NO. MPC-100(EU)-00

FOR PARTS OR SERVICE, ALWAYS GIVE COMPLETE SERVICE REF. NUMBER.



MSX type

64KB RAM

CONTENTS

WM-14975 Apr.,/'85/KO 100 Printed in Japan

SANYO ELECTRIC CO., LTD.
SANYO ELECTRIC TRADING CO., LTD.

1. SAFETY PRECAUTIONS

WARNING: The chassis of this apparatus is connected to one side of the AC line during operation, service should not be attempted by anyone not familiar with the precautions necessary when working on this type of equipment. The following precautions should be observed;

An isolation transformer should be connected in the power line between the set and the AC line before any service is performed on the set.

1. Comply with all caution and safety-related notes provided on cabinet, inside the cabinet, chassis or the peripheral devices.
2. When replacing a chassis in the cabinet, always be certain that all the protective devices are put back in the place, such as, nonmetallic control knobs, adjustment covers or shields, isolation resistor-capacitor networks etc.

Before returning any personal computer to the customer, the service technician must be sure that it is completely safe to operate without danger of electrical shock.

PRODUCT SAFETY NOTICE

Product safety should be considered when a component replacement is made in any area of a set. Components indicated by mark ⚠ in the parts list and the schematic diagram designate components in which safety can be of special significance. It is particularly recommended that only parts designated on the parts list in this manual be used for component replacement designated by mark ⚠. No deviations from resistance wattage or voltage ratings may be made for replacement items designated by mark ⚠.

2. SPECIFICATION

CPU	Z-80A Compatible (3.58 MHz)
Memory	MAIN MEMORY: 64 KB RAM SYSTEM MEMORY: 32 KB ROM VIDEO MEMORY: 16 KB RAM
Display	Text I: 24 Lines x 40 Characters, 16 colors Text II: 24 Lines x 32 Characters, 16 colors Graphic: 256 x 192 dots, 16 colors Multi Color: 64 x 48 blocks, 16 colors
Sound	3 Sound Channels, 8 octaves
Keyboard	73 Keys
Interface	Printer: 8 bit parallel (Centronics type) Cassette: FSK method, 1,200/2,400 bauds Joystick: 2 slots Cartridge Bus: 1 slot, 50 pin Expansion Bus: 1 slot, 50 pin
Output signal	Video 1.0 VP-P, 75 ohms, RCA phono jack Audio 1.26 VP-P, 600 ohms, RCA phono jack RF (UHF CH36, 591.25 MHz) RCA phono DIN 75 ohms plug
Dimensions	Cabinet: W385 x H62 x D242 (mm)
Weight	Net weight: 2.2 Kg
Power Supply	220V ~ 240V, AC 50/60 Hz
Power Consumption	11 watts

ACCESSORIES

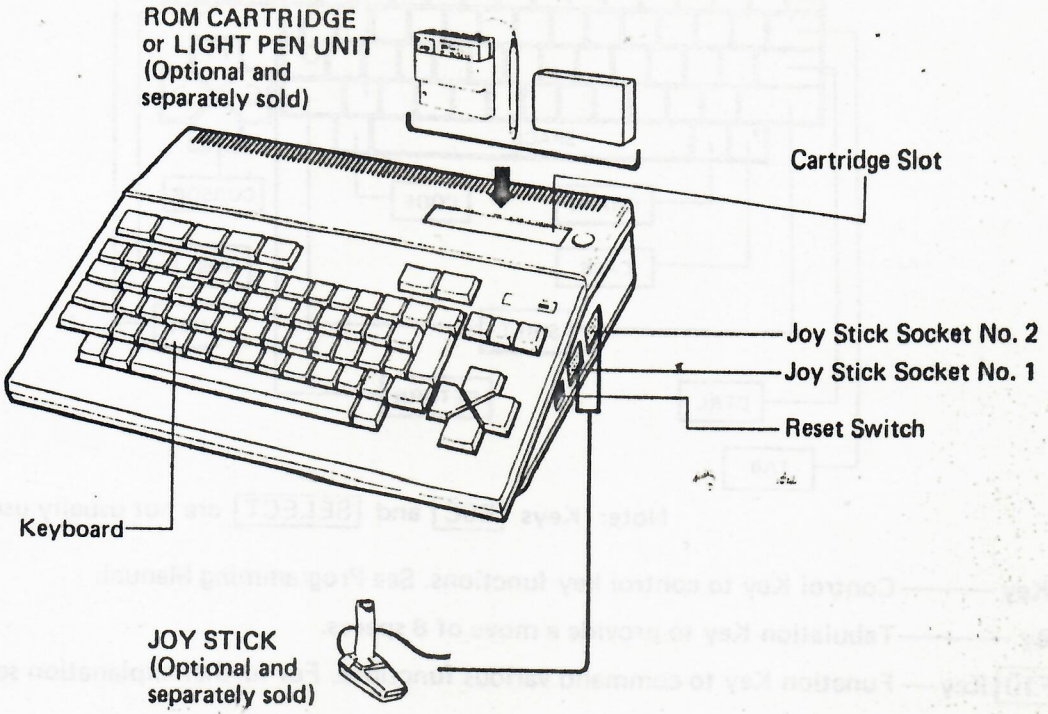
- RF cable
- Patch Cord for connecting to cassette tape recorder
- Operating Instructions
- Programming Manual

Apr. 1985

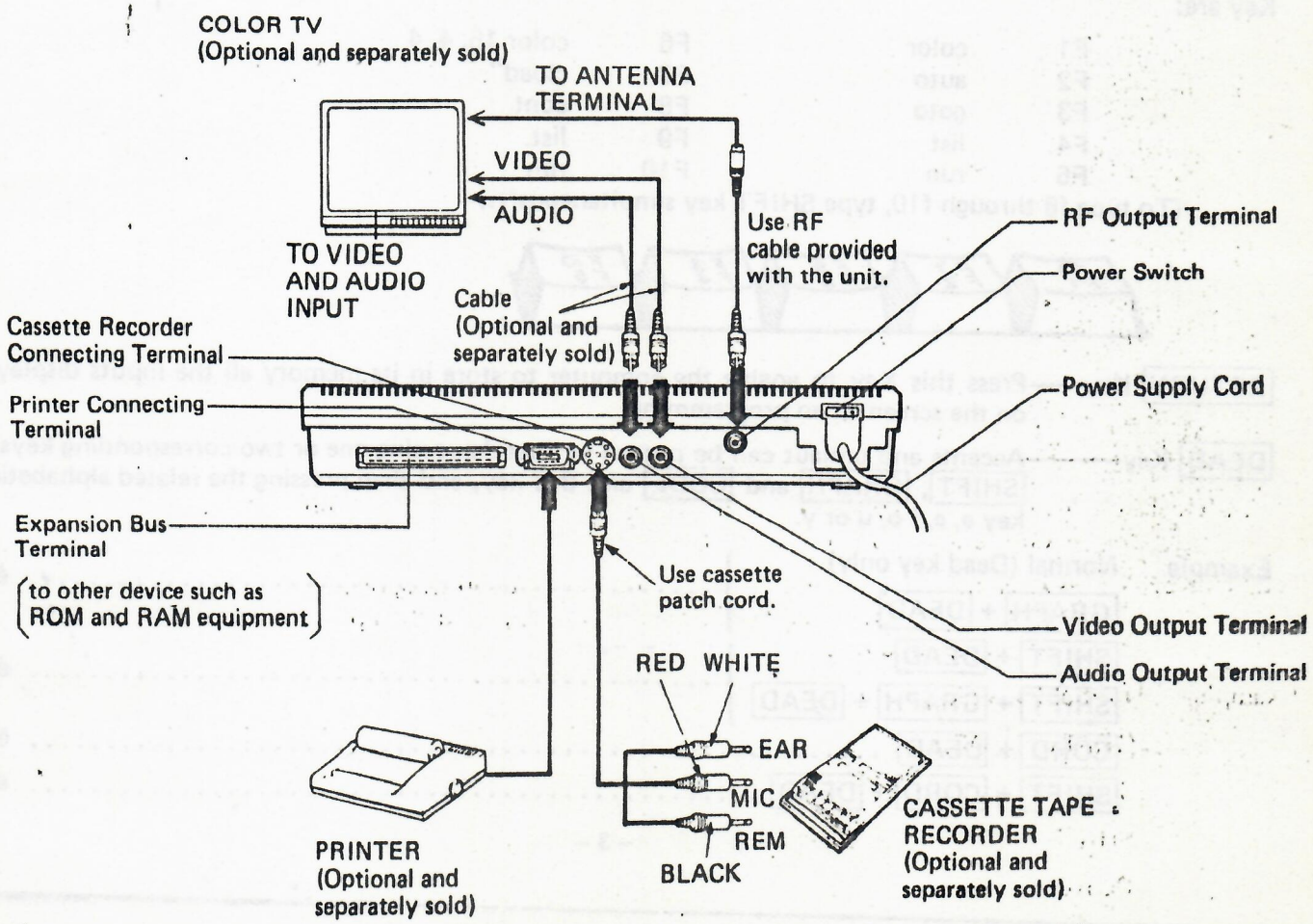
3. OPERATING SUMMARY

1. NAME OF PARTS AND CONNECTIONS

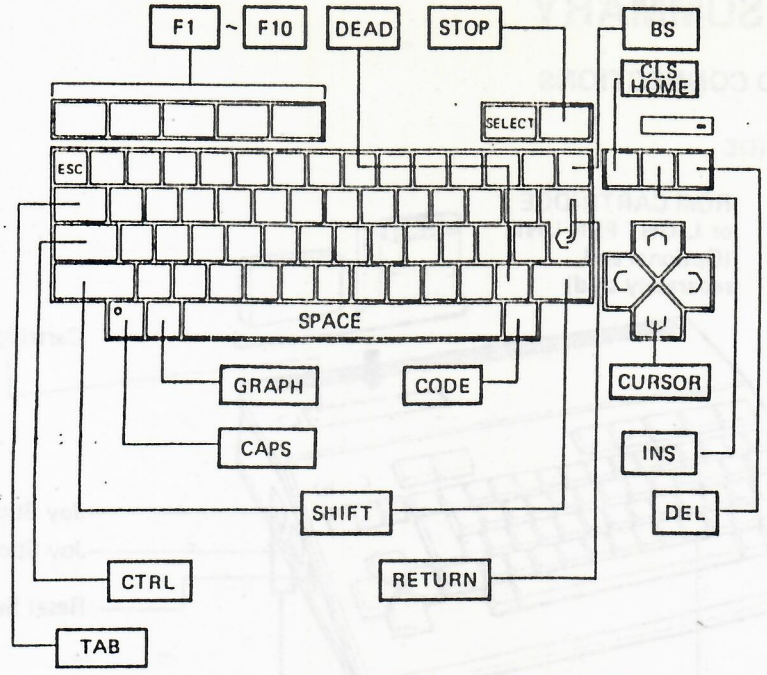
TOP AND RIGHT SIDE



REAR



2. KEY NAMES



Note: Keys [ESC] and [SELECT] are not usually used.

[CTRL] Key ——— Control Key to control key functions. See Programming Manual.

[TAB] Key ——— Tabulation Key to provide a move of 8 spaces.

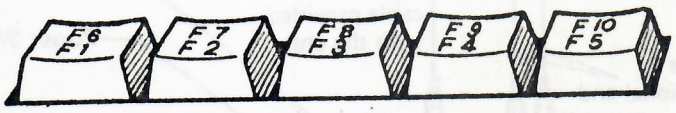
[F1] – [F10] Key — Function Key to command various functions. For further explanation see Note below.

Note:

This computer has 10 pre-defined Function Keys. The current contents of these Keys are displayed on the last line on the screen and can be redefined by program with KEY statement. The initial values for each Key are:

F1	color	F6	color 15, 4, 4
F2	auto	F7	cload"
F3	goto	F8	cont
F4	list	F9	list.
F5	run	F10	run

(To type f6 through f10, type SHIFT key simultaneously.)



[RETURN] Key — Press this Key to enable the computer to store in its memory all the inputs displayed on the screen when programming.

[DEAD] Key ——— Accents and umlaut can be put on by first depressing one or two corresponding keys of [SHIFT], [GRAPH] and [CODE] and this key, and then pressing the related alphabetical key a, e, i o, u or y.

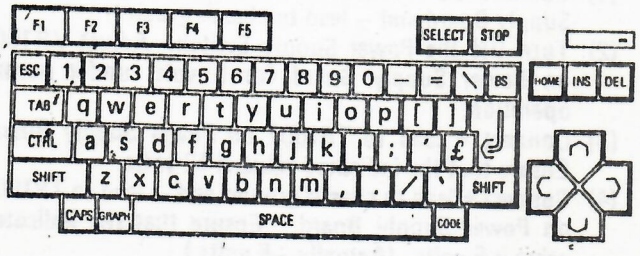
Example

Normal (Dead key only)	è, à
[GRAPH] + [DEAD]	
[SHIFT] + [DEAD]	é, á
[SHIFT] + [GRAPH] + [DEAD]	
[CORD] + [DEAD]	ê, â
[SHIFT] + [CORD] + [DEAD]	ë, ä

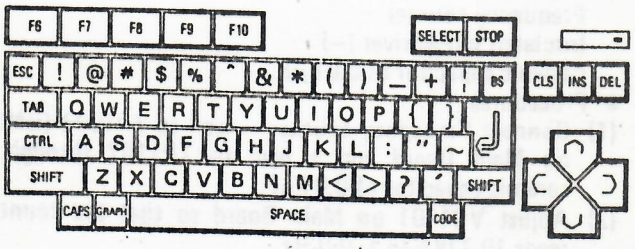
3. CHARACTERS AND SYMBOLS SET

The SHIFT, CAPS, GRAPH and CODE keys serve also to display the following characters and graphic symbols on the screen.

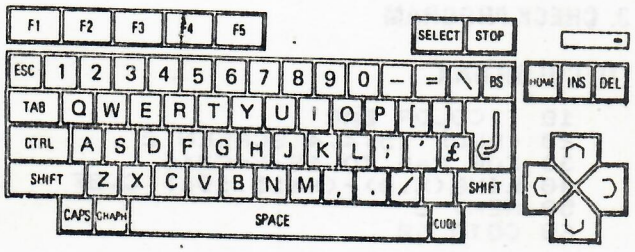
1. NORMAL KEYBOARD



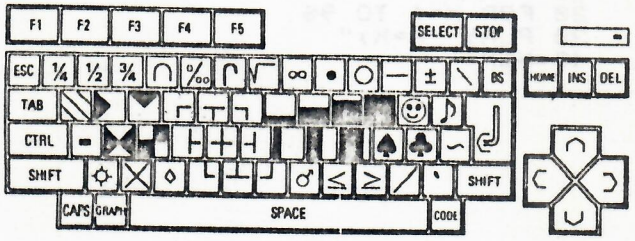
2. SHIFT + ANY KEY



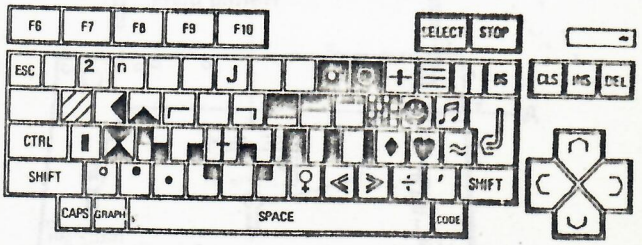
3. CAPS ⊕ ANY KEY



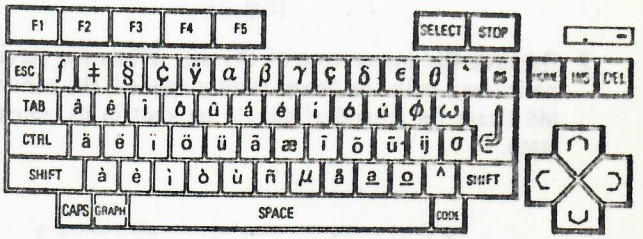
4. GRAPH + ANY KEY



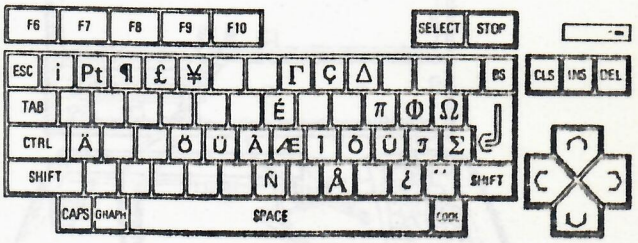
5. GRAPH + SHIFT + ANY KEY



6. CODE + ANY KEY



7. CODE + SHIFT + ANY KEY



Note:

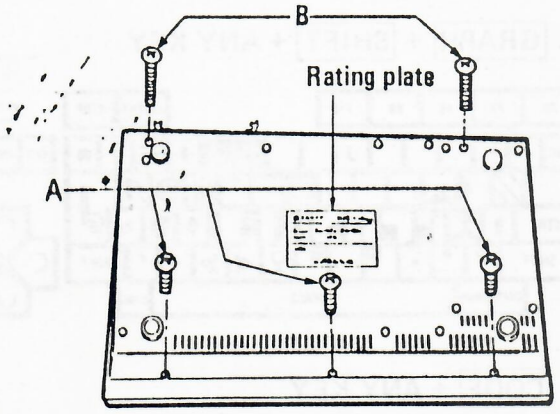
The mark ⊕ in the key explanation means a toggle key.
Example: CAPS ⊕

The mark + denotes that one key is pushed down with its preceding key kept depressed.
Example: SHIFT + A
(Push A key while keeping SHIFT key down.)

4. MECHANICAL DISASSEMBLY INSTRUCTIONS

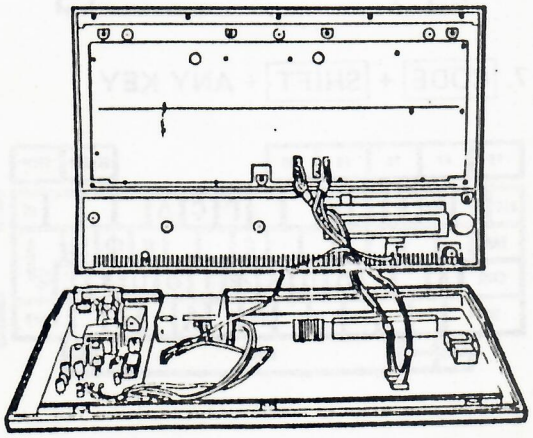
1. CABINET DISASSEMBLY

1. Remove three screws (A) and two screws (B).



(Fig. 1)

2. Remove the upper case of the set. When the service is performed with the power supply applied, the connector MS (reset for cartridge) should be kept in its connected state.



(Fig. 2)

3. When installing, align the positions of the Power Supply cord and RF-Video Modulator properly.

2. POWER SUPPLY UNIT REMOVAL

The power supply unit can be removed from the lower case by removing the four attaching screws.

5. INSTALLATION AND SERVICE ADJUSTMENT

1. ADJUSTMENT OF POWER SUPPLY VOLTAGE (VR1001)

- Adjustment equipment:
  DC Voltmeter (internal registance: 20 kΩ minimum)
  Insulated screwdriver (–)
- Procedures

(1) Connect DC Voltmeter + lead to TP1001 on Power Supply Board and – lead to chassis ground.
(2) Turn ON the Power Supply Switch. Adjust VR1001 on Power Supply Board for 5 volts under normal operation.
(3) Connect + lead to TP1002 on Power Supply Board. Ensure that the indicated value is 12 volts.
(4) Connect + lead to chassis ground and – lead to TP1003 on Power Supply Board. Ensure that the indicated value is 5 volts. (Actually –5 volts.)

2. VDP CLOCK ADJUSTMENT (VC1101)

- Adjustment equipment:
  Frequency counter
  Insulated screwdriver (–)
  Ceramic capacitor of 0.01 μF.
- Procedures

(1) Connect Frequency counter – lead to TP1002 (GND) on Main Board and + lead to TP1107 through a ceramic capacitor of 0.01 μF.
(2) Adjust VC1101 on Main Board so that the counter reads 10,738,635 ± 150 Hz.
(3) After completion of the adjustment, remove the counter and capacitor.

3. CHECK PROGRAM

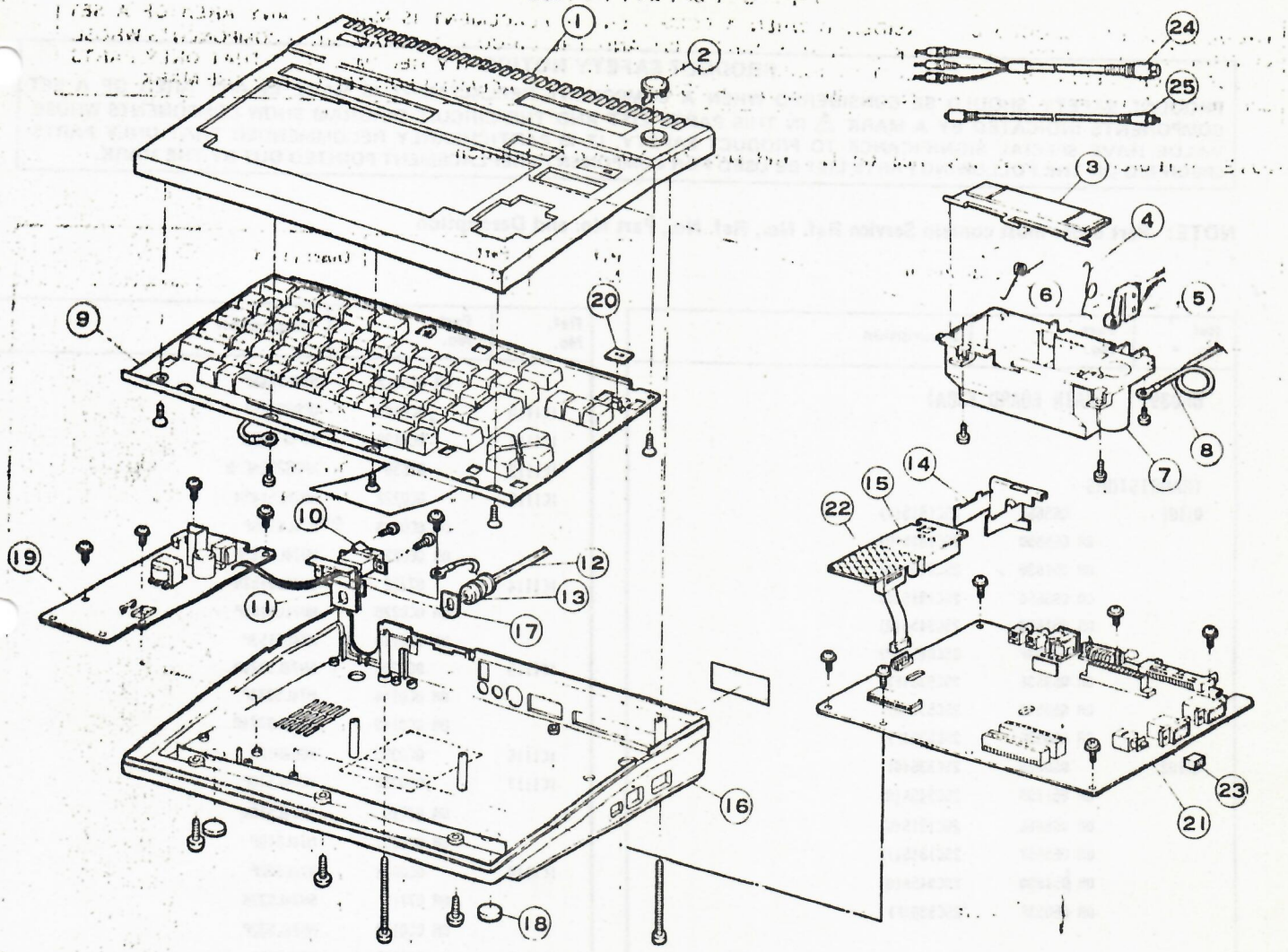
(1) COLOR BAR

```
10 ' COLOR BAR
20 COLOR 15,4,4:SCREEN 2
30 FOR C=0 TO 15:X=C*16
40 LINE(X,0)-(X+15,191),C,BF
50 NEXT C
60 GOTO 60
```

(2) SOUND OUTPUT

```
10 ' PLAY
20 FOR X=1 TO 96
30 PLAY "N=X;"
40 NEXT
```

1. MECHANICAL PARTS LIST



Key No.	Part No.	Description
1.	3M02156	Cabinet, Top
2.	3M01175	Cap
3.	3M01128	Cartridge Door
	1S00093	Spring, Power Switch Mtg.
o.	————	Reset Switch (See chassis electrical parts list)
6.	1S00092	Spring, Cartridge Door Mtg.
7.	3M01129	Cartridge Holder
	NBS3010E	Screw 3 x 10mm, Cartridge Holder Mtg. (3 used)
8.	3M01325	Wire Holder
9.	————	Keyboard Assembly
	NUS3008E	Screw 3 x 8mm, Keyboard Mtg. (6 used)
	or NUS3008EB	
	NBS3008E	Screw 3 x 8mm, Keyboard Mtg.
10.	————	Power Switch (See chassis electrical parts list)
	NBS3008E	Screw 3 x 8mm, Power Switch Mtg. (2 used)
11.	1P01107	Power Switch Mtg. Plate
	NBS3008E	Screw 3 x 8mm, Power Switch Mtg. Plate
12.	————	AC Power Cord (See chassis electrical parts list)
13.	3M03675	Bush, AC Power Cord Mtg.
14.	1P01106	RF-Video Modulator
	————	RF-Video Modulator

Key No.	Part No.	Description
16.	3M02112	Cabinet, Bottom
	NBS4012E	Screw 4 x 12mm, Cabinet Mtg. (3 used)
	1650010	Screw 4 x 45mm, Cabinet Mtg. (2 used)
	3P03363	Caution Label, Rear
	3P03740	Rating Plate
	3P03492	Caution Label, Bottom
17.	3S01381	Insulation Sheet
18.	3R00326	Cushion, Bottom Cabinet (2 used)
19.	————	Power Board (See chassis electrical parts list)
	160366	Screw 3 x 8mm, Power Board Mtg. (4 used)
20.	3S01122	Spacer, Power Indicator
21.	————	Main Board (See chassis electrical parts list)
	160366	Screw 3 x 8mm, Main Board Mtg. (5 used)
	NBS3010E	Screw 3 x 10mm, Main Board Mtg.
	NNS3008E	Screw 3 x 8mm, Printer Socket Mtg.
	NRS3000	Nut 3mm, Printer Socket Mtg.
22.	3201763	Insulation Sheet, RF-Video Modulator
23.	3M01174	Reset Button
24.	EW0034	Cassette Patch Cord
25.	EW0076	RF Cable
	3P02945	Owner's Manual
	3P02813	Programming Manual

2. ELECTRICAL PARTS LIST

PRODUCT SAFETY NOTICE

PRODUCT SAFETY SHOULD BE CONSIDERED WHEN A COMPONENT REPLACEMENT IS MADE IN ANY AREA OF A SET COMPONENTS INDICATED BY A MARK ⚠ IN THIS PARTS LIST AND THE CIRCUIT DIAGRAM SHOW COMPONENTS WHOSE VALUE HAVE SPECIAL SIGNIFICANCE TO PRODUCT SAFETY. IT IS PARTICULARLY RECOMMENDED THAT ONLY PARTS SPECIFIED ON THE FOLLOWING PARTS LIST BE USED FOR COMPONENTS REPLACEMENT POINTED OUT BY THE MARK.

NOTE: Part order must contain Service Ref. No., Ref. No., Part No. and Description

Ref. No.	Part No.	Description
UF0397 (MAIN BOARD Y3BA)		
TRANSISTORS		
Q1101	Q6565Y	2SC1815(Y)
	OR Q6565O	2SC1815(O)
	OR Q5183Q	2SC945A(Q)
	OR Q6565G	2SC1815(G)
	OR Q5183R	2SC945A(R)
	OR Q5183P	2SC945A(P)
	OR Q5053E	2SC536(E)
	OR Q5053G	2SC536(G)
	OR Q5053F	2SC536(F)
Q1102	Q5053G	2SC536(G)
	OR Q5183R	2SC945A(R)
	OR Q6565G	2SC1815(G)
	OR Q6565Y	2SC1815(Y)
	OR Q5183Q	2SC945A(Q)
	OR Q5053F	2SC536(F)
INTEGRATED CIRCUITS		
IC1101	Q7089	SN7404
	OR QC0115	M53204P
	OR QC0136	HD7404P
IC1103	QC0113	M74LS367AP
	OR QC0148	HD74LS367AP
	OR QC0202	SN74LS367AN
IC1104	QC0146	HD74LS157P
	OR QC0111	M74LS157P
	OR QC0021	SN74LS157N
IC1105	QC0021	SN74LS157N
	OR QC0146	HD74LS157P
	OR QC0111	M74LS157P
IC1106	Q7170	M53207P
	OR QC0195	SN7407N
	OR QC0137	HD7407P
IC1107	QC0140	HD74LS04P
	OR Q7707	SN74LS04N
	OR Q7251	M74LS04P
IC1108	QC0108	M74LS14P
	OR QC0142	HD74LS14P
	OR Q7712	SN74LS14N
IC1109	Q7731	SN74LS245N
	OR QC0147	HD74LS245WP
	OR QC0112	M74LS245P
IC1110	QC0123	UPD780C-1
IC1111	QC0130	AY-3-8910
IC1112	Q7698	UPD8255AC-5
IC1113	QC0222	SN74LS145N
	OR QC0223	M74LS145P
	OR QC0221	HD74LS145P
IC1114	Q7722	SN74LS153N
	OR QC0220	HD74LS153P
	OR QC0219	M74LS153P
IC1115	QC0203	SN74LS374N
	OR QC0114	M74LS374P
	OR QC0149	HD74LS374P
IC1116	QC0399	MB64H120
IC1117	QC0286	HD74LS10P
	OR Q7710	SN74LS10N
	OR QC0287	M74LS10P
IC1118	QC0044	M74LS32P
	OR Q7717	SN74LS32N
	OR QC0174	HD74LS32P
IC1119	QC0027	M74LS00P
	OR Q7214	SN74LS00
	OR QC0173	HD74LS00P
IC1122	QC0564	HN613256PH80
IC1123	Q7709	SN74LS08N
	OR QC0141	HD74LS08P
	OR Q7445	M74LS08P
IC1124	Q7717	SN74LS32N
	OR QC0174	HD74LS32P
	OR QC0044	M74LS32P
IC1126	QC0140	HD74LS04P
	OR Q7251	M74LS04P
	OR Q7707	SN74LS04N
IC1127	QC0143	HD74LS74AP
	OR Q7447	M74LS74AP
	OR Q7718	SN74LS74AN
IC1128	QC0021	SN74LS157N
	OR QC0146	HD74LS157P
	OR QC0111	M74LS157P
IC1129	QC0021	SN74LS157N
	OR QC0111	M74LS157P
	OR QC0146	HD74LS157P

Ref. No.	Part No.	Description
IC1130	Q7718	SN74LS74AN
	OR Q7447	M74LS74AP
	OR QC0143	HD74LS74AP
IC1131	QC0143	HD74LS74AP
	OR Q7718	SN74LS74AN
	OR Q7447	M74LS74AP
IC1132	QC0337	M5K4164AP-15
	OR QC0307	M5K4164ANP-15
	OR QC0339	HM4864P-2
	OR QC0340	HM4864AP-15
	OR QC0574	MB8264A-15P
IC1133	QC0337	M5K4164AP-15
	OR QC0307	M5K4164ANP-15
	OR QC0339	HM4864P-2
	OR QC0340	HM4864AP-15
	OR QC0574	MB8264A-15P
IC1134	QC0337	M5K4164AP-15
	OR QC0307	M5K4164ANP-15
	OR QC0339	HM4864P-2
	OR QC0340	HM4864AP-15
	OR QC0574	MB8264A-15P
IC1135	QC0337	M5K4164AP-15
	OR QC0307	M5K4164ANP-15
	OR QC0339	HM4864P-2
	OR QC0340	HM4864AP-15
	OR QC0574	MB8264A-15P
IC1136	QC0337	M5K4164AP-15
	OR QC0307	M5K4164ANP-15
	OR QC0339	HM4864P-2
	OR QC0340	HM4864AP-15
	OR QC0574	MB8264A-15P
IC1137	QC0337	M5K4164AP-15
	OR QC0307	M5K4164ANP-15
	OR QC0339	HM4864P-2
	OR QC0340	HM4864AP-15
	OR QC0574	MB8264A-15P
IC1138	QC0337	M5K4164AP-15
	OR QC0307	M5K4164ANP-15
	OR QC0339	HM4864P-2
	OR QC0340	HM4864AP-15
	OR QC0574	MB8264A-15P
IC1139	QC0337	M5K4164AP-15
	OR QC0307	M5K4164ANP-15
	OR QC0339	HM4864P-2
	OR QC0340	HM4864AP-15
	OR QC0574	MB8264A-15P
IC1140	QC0544	TMS9929ANL
IC1141	QC0232	UPD416C-2
	OR QC0251	TMM416P-3
IC1142	QC0232	UPD416C-2
	OR QC0251	TMM416P-3
IC1143	QC0232	UPD416C-2
	OR QC0251	TMM416P-3
IC1144	QC0232	UPD416C-2
	OR QC0251	TMM416P-3

Ref. No.	Part No.	Description
IC1145	QC0232	UPD416C-2
	OR QC0251	TMM416P-3
IC1146	QC0232	UPD416C-2
	OR QC0251	TMM416P-3
IC1147	QC0232	UPD416C-2
	OR QC0251	TMM416P-3
IC1148	QC0232	UPD416C-2
	OR QC0251	TMM416P-3

CAPACITORS

C1101	CCHBJ5R0	CERAMIC, 5PF, +-5%, 50V
C1102	CFHMJ103	MYLAR FILM, 0.01MF, +-5%, 50V
C1103	CEBEM470	ELECTROLYTIC, 47MF, 10V
C1104	CFHBJ104	MYLAR FILM, 0.1MF, 50V
C1105	CFHBJ104	MYLAR FILM, 0.1MF, +-5%, 50V
C1106	CFHBJ104	MYLAR FILM, 0.1MF, +-5%, 50V
C1107	CFHBJ104	MYLAR FILM, 0.1MF, +-5%, 50V
C1108	CFHBJ104	MYLAR FILM, 0.1MF, +-5%, 50V
C1109	CFHBJ104	MYLAR FILM, 0.1MF, +-5%, 50V
C1110	CFHBJ104	MYLAR FILM, 0.1MF, +-5%, 50V
C1111	CEBFM220	ELECTROLYTIC, 22MF, 10V
C1112	CFHBJ104	MYLAR FILM, 0.1MF, +-5%, 50V
C1113	CFHBJ104	MYLAR FILM, 0.1MF, +-5%, 50V
C1114	CFHBJ104	MYLAR FILM, 0.1MF, +-5%, 50V
C1115	CFHBJ104	MYLAR FILM, 0.1MF, +-5%, 50V
C1116	CFHBJ104	MYLAR FILM, 0.1MF, +-5%, 50V
C1117	CFHBJ104	MYLAR FILM, 0.1MF, +-5%, 50V
C1118	CEBEM221	ELECTROLYTIC, 220MF, 10V
C1119	CEFAN1R0	NON-POLARIZED ELECTROLYTIC, 1MF, 25V
C1120	CEFAN1R0	NON-POLARIZED ELECTROLYTIC, 1MF, 25V
C1121	CEBEM221	ELECTROLYTIC, 220MF, 10V
C1122	CEBEM220	ELECTROLYTIC, 22MF, 10V
C1123	CFHBJ104	MYLAR FILM, 0.1MF, +-5%, 50V
C1124	CEBEM220	ELECTROLYTIC, 22MF, 10V
C1125	CEFEM220	ELECTROLYTIC, 22MF, 25V
C1126	CFHBJ104	MYLAR FILM, 0.1MF, +-5%, 50V
C1127	CFHBJ104	MYLAR FILM, 0.1MF, +-5%, 50V
C1128	CFHBJ104	MYLAR FILM, 0.1MF, +-5%, 50V
C1129	CFHBJ104	MYLAR FILM, 0.1MF, +-5%, 50V
C1130	CFHBJ104	MYLAR FILM, 0.1MF, +-5%, 50V
C1131	CFHBJ104	MYLAR FILM, 0.1MF, +-5%, 50V
C1132	CFHBJ104	MYLAR FILM, 0.1MF, +-5%, 50V
C1134	CEFEM220	ELECTROLYTIC, 22MF, 25V
C1135	CFHBJ104	MYLAR FILM, 0.1MF, +-5%, 50V
C1136	CFHBJ104	MYLAR FILM, 0.1MF, +-5%, 50V
C1137	CFHBJ104	MYLAR FILM, 0.1MF, +-5%, 50V
C1138	CFHBJ104	MYLAR FILM, 0.1MF, +-5%, 50V
C1141	C9606	CERAMIC, 0.1MF, +80%-20%, 50V
C1142	C9606	CERAMIC, 0.1MF, +80%-20%, 50V
C1143	C9606	CERAMIC, 0.1MF, +80%-20%, 50V
C1144	C9606	CERAMIC, 0.1MF, +80%-20%, 50V
C1145	C9606	CERAMIC, 0.1MF, +80%-20%, 50V
C1146	C9606	CERAMIC, 0.1MF, +80%-20%, 50V
C1147	C9606	CERAMIC, 0.1MF, +80%-20%, 50V

Ref. No.	Part No.	Description
C1148	C9606	CERAMIC, 0.1MF, +80%-20%, 50V
C1149	C9606	CERAMIC, 0.1MF, +80%-20%, 50V
C1150	C9606	CERAMIC, 0.1MF, +80%-20%, 50V
C1151	C9606	CERAMIC, 0.1MF, +80%-20%, 50V
C1152	C9606	CERAMIC, 0.1MF, +80%-20%, 50V
C1153	C9606	CERAMIC, 0.1MF, +80%-20%, 50V
C1154	C9606	CERAMIC, 0.1MF, +80%-20%, 50V
C1155	C9606	CERAMIC, 0.1MF, +80%-20%, 50V
C1156	CFHBJ104	MYLAR FILM, 0.1MF, +-5%, 50V
C1157	CEBEM471	ELECTROLYTIC, 470MF, 10V
C1158	C9606	CERAMIC, 0.1MF, +80%-20%, 50V
C1159	C9606	CERAMIC, 0.1MF, +80%-20%, 50V
C1160	C9606	CERAMIC, 0.1MF, +80%-20%, 50V
C1161	C9606	CERAMIC, 0.1MF, +80%-20%, 50V
C1162	C9606	CERAMIC, 0.1MF, +80%-20%, 50V
C1163	C9606	CERAMIC, 0.1MF, +80%-20%, 50V
C1164	C9606	CERAMIC, 0.1MF, +80%-20%, 50V
C1165	C9606	CERAMIC, 0.1MF, +80%-20%, 50V
C1166	C9606	CERAMIC, 0.1MF, +80%-20%, 50V
C1167	C9606	CERAMIC, 0.1MF, +80%-20%, 50V
C1168	C9606	CERAMIC, 0.1MF, +80%-20%, 50V
C1169	C9606	CERAMIC, 0.1MF, +80%-20%, 50V
C1170	C9606	CERAMIC, 0.1MF, +80%-20%, 50V
C1171	C9606	CERAMIC, 0.1MF, +80%-20%, 50V
C1172	C9606	CERAMIC, 0.1MF, +80%-20%, 50V
C1173	CFHBJ104	MYLAR FILM, 0.1MF, +-5%, 50V
C1175	CEBEM471	ELECTROLYTIC, 470MF, 10V
C1176	CCHFJ681	CERAMIC, 680PF, +-5%, 50V
C1178	CCHBJ101	CERAMIC, 100PF, +-5%, 50V
C1179	CCHBJ101	CERAMIC, 100PF, +-5%, 50V
RESISTORS		
RN1101	RN0035	RESISTOR BLOCK, 10K x 8P
RN1102	RN0035	RESISTOR BLOCK, 10K x 8P
RN1103	RN0035	RESISTOR BLOCK, 10K x 8P
R1101	RFACJ681	CARBON, 680 OHM, +-5%, 1/4W
R1102	RFACJ681	CARBON, 680 OHM, +-5%, 1/4W
R1103	RFACJ220	CARBON, 22 OHM, +-5%, 1/4W
R1104	RFACJ101	CARBON, 100 OHM, +-5%, 1/4W
R1105	RFACJ562	CARBON, 5600 OHM, +-5%, 1/4W
R1106	RFACJ562	CARBON, 5600 OHM, +-5%, 1/4W
R1107	RFACJ562	CARBON, 5600 OHM, +-5%, 1/4W
R1108	RFACJ562	CARBON, 5600 OHM, +-5%, 1/4W
R1109	RFACJ472	CARBON, 4700 OHM, +-5%, 1/4W
R1110	RFACJ391	CARBON, 390 OHM, +-5%, 1/4W
R1111	RFACJ391	CARBON, 390 OHM, +-5%, 1/4W
R1112	RFACJ331	CARBON, 330 OHM, +-5%, 1/4W
R1113	RFACJ103	CARBON, 10K OHM, +-5%, 1/4W
R1114	RFACJ472	CARBON, 4700 OHM, +-5%, 1/4W
R1115	RFACJ472	CARBON, 4700 OHM, +-5%, 1/4W
R1116	RFACJ101	CARBON, 100 OHM, +-5%, 1/4W
R1117	RFACJ472	CARBON, 4700 OHM, +-5%, 1/4W
R1118	RFACJ102	CARBON, 1K OHM, +-5%, 1/4W
R1119	RFACJ472	CARBON, 4700 OHM, +-5%, 1/4W
R1120	RFACJ220	CARBON, 22 OHM, +-5%, 1/4W
VR1103	RFACJ471	CARBON, 470 OHM, +-5%, 1/4W

Ref. No.	Part No.	Description
R1121	RFACJ102	CARBON, 1K OHM, +-5%, 1/4W
R1122	RFACJ561	CARBON, 560 OHM, +-5%, 1/4W
R1123	RFBPJ151	CARBON, 150 OHM, +-5%, 1/2W
R1124	RFACJ472	CARBON, 4700 OHM, +-5%, 1/4W
R1125	RFACJ472	CARBON, 4700 OHM, +-5%, 1/4W
R1126	RFACJ220	CARBON, 22 OHM, +-5%, 1/4W
R1127	RFACJ220	CARBON, 22 OHM, +-5%, 1/4W
R1130	RFACJ472	CARBON, 4700 OHM, +-5%, 1/4W
R1135	RFACJ750	CARBON, 75 OHM, +-5%, 1/4W
R1138	RFACJ473	CARBON, 47K OHM, +-5%, 1/4W
R1139	RFACJ103	CARBON, 10K OHM, +-5%, 1/4W
R1140	RFACJ103	CARBON, 10K OHM, +-5%, 1/4W
R1141	RFACJ471	CARBON, 470 OHM, +-5%, 1/4W
R1143	RFJCJ102	CARBON, 1K OHM, +-5%, 1/6W
R1144	RFJCJ102	CARBON, 1K OHM, +-5%, 1/6W
R1145	RFACJ681	CARBON, 680 OHM, +-5%, 1/4W
R1146	RFACJ681	CARBON, 680 OHM, +-5%, 1/4W
COILS		
L1115	LDAK8R2	PEAKING, 8.2MH
L1116	LDAK8R2	PEAKING, 8.2MH
L1117	LDAK151	PEAKING COIL, 150MH
DIODES		
D1101	E1775R	DS442
	OR E1324R	1S2076
	OR E1229R	1S2473
	OR E1121R	1S1555
D1102	E1121R	1S1555
	OR E1229R	1S2473
	OR E1324R	1S2076
	OR E1775R	DS442
D1103	E1775R	DS442
	OR E1324R	1S2076
	OR E1229R	1S2473
	OR E1121R	1S1555
D1104	E1121R	1S1555
	OR E1229R	1S2473
	OR E1324R	1S2076
	OR E1775R	DS442
D1105	E1324R	1S2076
	OR E1229R	1S2473
	OR E1121R	1S1555
	OR E1775R	DS442
D1106	E1775R	DS442
	OR E1229R	1S2473
	OR E1324R	1S2076
	OR E1121R	1S1555
D1107	E1121R	1S1555
	OR E1775R	DS442
	OR E1324R	1S2076
	OR E1229R	1S2473
D1108	E1031RT	1S188TV
D1109	E1031RT	1S188TV

Ref. No.	Part No.	Description
D1110	E1031RT	1S188TV
D1111	E1031RT	1S188TV
D1112	E1031RT	1S188TV
D1113	E1031RT	1S188TV
D1114	E1229R	1S2473
	OR E1775R	DS442
	OR E1324R	1S2076
	OR E1121R	1S1555
D1115	E1121R	1S1555
	OR E1775R	DS442
	OR E1324R	1S2076
	OR E1229R	1S2473
D1116	E1229R	1S2473
	OR E1775R	DS442
	OR E1324R	1S2076
	OR E1121R	1S1555
D1117	ED0061D	EQA02-05D
D1118	E1121R	1S1555
	OR E1775R	DS442
	OR E1324R	1S2076
	OR E1229R	1S2473

MISCELLANEOUS

IC1121A	EK0160	IC SOCKET, 28P (SERVICE REF. NO. MPC-100-00 ONLY)
IC1122A	EK0160	IC SOCKET, 28P (SERVICE REF. NO. MPC-100-00 ONLY)
IC1140A	EK0020	IC SOCKET, 40P

MISCELLANEOUS

A1101	JU0067	SOUND I/F MODULATOR
KHBS	EK0084W	JACK, RCA, 1P
KHCS	EK0084Y	JACK, RCA, 1P
KHDS	E3347	DIN SOCKET, 8P
KHES	EK0136	SOCKET, 14P, PRINTER
KHFP	EK0171	PLUG, 50P, EXPANSION BUS
KHGS	EK0170	SOCKET, 50P, CARTRIDGE SLOT
	OR EK0170A	SOCKET, 50P, CARTRIDGE SLOT
KHIP	EK0172	PLUG, 9P, JOY STICK
KHJP	EK0172	PLUG, 9P, JOY STICK
KHNP	E39008	HOUSING, 9P
KHOP	E3947	CONNECTOR, 4P
KHPS	EK0341	CONNECTOR, 16P, KEYBOARD LEAD
KHQS	EK0341	CONNECTOR, 16P, KEYBOARD LEAD
KHSP	E3985	HOUSING, 3P
KHTP	E39014	HOUSING PLUG, 2P
RL1101	EF0023	RELAY, DC12V
SW1101	ES0077	SWITCH, RESET
VC1101	C9026	TRIMMER CAPACITOR, 4-30PF
X1101	EX0027XC	CRYSTAL, 10.738635MHZ

Ref. No.	Part No.	Description

UF0399 (POWER BOARD Y38A)

TRANSISTORS

Q1001	Q6556F	2SC2274(F)
	OR Q6556E	2SC2274K(E)
Q1002	QT0138ZY	2SD1571
Q1050	QT0073S	2SB892(S)
	OR QT0073T	2SB892(T)
Q1051	Q5053G	2SC536(G)
	OR Q5053F	2SC536(F)
Q1053	Q5053G	2SC536(G)
	OR Q5053F	2SC536(F)

INTEGRATED CIRCUITS

⚠ IC1001	QC0042L	L78M12-LU
⚠ IC1002	QC0264A	TL431C-LPB
	OR QC0264	TL431C-LP
⚠ IC1003	QC0236A	L78N12

CAPACITORS

⚠ C1001	CFUBM104	MYLAR FILM, 0.1MF, +-20%, 630V
⚠ C1002	CC0006	CERAMIC, 1000PF, +-20%, 400V
C1005	CFHSK153	MYLAR FILM, 0.015MF, +-10%, 50V
	OR CFHRK153	MYLAR FILM, 0.015MF, +-10%, 50V
C1006	CFHSK562	MYLAR FILM, 5600PF, +-10%, 50V
	OR CFHRK562	MYLAR FILM, 5600PF, +-10%, 50V
C1007	CFHBJ474	MYLAR FILM, 0.47MF, +-5%, 50V
C1008	CEHEM330	ELECTROLYTIC, 33MF, 50V
C1009	CCZSK331	CERAMIC, 330PF, +-10%, 2KV
C1010	CE0061	ELECTROLYTIC, 47MF, +-20%, 400V
C1011	CFHSK473	MYLAR FILM, 0.047MF, +-10%, 50V
	OR CFHRK473	MYLAR FILM, 0.047MF, +-10%, 50V
C1014	CEBEM102	ELECTROLYTIC, 1000MF, 10V
C1015	CEBEM102	ELECTROLYTIC, 1000MF, 10V
C1016	CEBEM102	ELECTROLYTIC, 1000MF, 10V
C1017	CEBEM471	ELECTROLYTIC, 470MF, 10V
C1018	CEGEM221	ELECTROLYTIC, 220MF, 35V
C1019	CEDEM470	ELECTROLYTIC, 47MF, 16V
C1020	CEFEM221	ELECTROLYTIC, 220MF, 25V
C1021	CEDEM470	ELECTROLYTIC, 47MF, 16V
C1024	CFHSK223	MYLAR FILM, 0.022MF, +-10%, 50V
	OR CFHRK223	MYLAR FILM, 0.022MF, +-10%, 50V
C1025	CEHEM4R7	ELECTROLYTIC, 4.7MF, 50V
⚠ C1030	CC0006	CERAMIC, 1000PF, +-20%, 400V
C1050	CFHRK154	MYLAR FILM, 0.15MF, +-10%, 50V

RESISTORS

R1001	RY5KK100	WIRE WOUND, 10 OHM, +-10%, 5W
R1002	RFBPJ394	CARBON, 390K OHM, +-5%, 1/2W
R1003	RNBPJ221	METALIZED CARBON, 220 OHM, +-5%, 1/2W
R1004	RFAZJ100	CARBON, 10 OHM, +-5%, 1/4W
R1005	RFAAJ472	CARBON, 4700 OHM, +-5%, 1/4W

Ref. No.	Part No.	Description
R1006	RFAZJ101	CARBON, 100 OHM, +-5%, 1/4W
R1007	RY2PJ3R9	WIRE WOUND, 3.9 OHM, +-5%, 2W
R1008	RR2FJ331	OXIDE METALIZED, 330 OHM, +-5%, 2W
R1010	RFJCJ102	CARBON, 1K OHM, +-5%, 1/6W
R1011	RFJCJ152	CARBON, 1500 OHM, +-5%, 1/6W
R1012	RFACJ470	CARBON, 47 OHM, +-5%, 1/4W
R1013	RFJCJ272	CARBON, 2700 OHM, +-5%, 1/6W
R1016	RFAAJ102	CARBON, 1K OHM, +-5%, 1/4W
R1017	RFAAJ1R0	CARBON, 1 OHM, +-5%, 1/4W
R1019	RFBPJ224	CARBON, 220K OHM, +-5%, 1/2W
R1020	RFAAJ1R0	CARBON, 1 OHM, +-5%, 1/4W
R1021	RFBAJ1R0	CARBON, 1 OHM, +-5%, 1/2W
R1023	RFAAJ1R0	CARBON, 1 OHM, +-5%, 1/4W
R1050	RFBPJ102	CARBON, 1K OHM, +-5%, 1/2W
R1051	RFJCJ222	CARBON, 2200 OHM, +-5%, 1/6W
R1052	RFJCJ121	CARBON, 120 OHM, +-5%, 1/6W
R1053	RFJCJ101	CARBON, 100 OHM, +-5%, 1/6W
R1054	RFJCJ331	CARBON, 330 OHM, +-5%, 1/6W
R1057	RFJCJ101	CARBON, 100 OHM, +-5%, 1/6W
R1060	RR2FJ5R6	OXIDE METALIZED, 5.6 OHM, +-5%, 2W
VARIABLE RESISTORS		
⚠ VR1001	GF0109DT	1K OHM, +5V ADJ
TRANSFORMERS		
⚠ T1001	AE0040	CONVERTOR
COILS		
⚠ L1001	LQ0011	LINE FILTER
L1002	L4056	INDUCTOR, 47MH
DIODES		
⚠ D1001	ED0208	RB-15C
D1002	ED0089	1SS132
OR	ED0088	1SS177
OR	ED0087	GMA01
D1003	ED0071	A21-04
OR	ED0070	EU01
D1004	ED0061D	EQA02-05D
D1005	ED0032	1SS176
D1007	ED0070	EU01
OR	ED0071	A21-04
D1008	E1786R	EU2
D1009	ED0205XS	RK44LF-K2
⚠ D1013	EL0065G	PHOTO COUPLER, TLP632-GB
D1014	E1790R	B12-02R
D1015	E1790R	B12-02R

Ref. No.	Part No.	Description
MISCELLANEOUS		
⚠ F1001	E5045	FUSE, T2A, AC
F1001A	E5740	FUSE CLIP
F1001B	E5740	FUSE CLIP
⚠ F1002	E5108	FUSE, T4A, 250V
F1002A	E5740	FUSE CLIP
F1002B	E5740	FUSE CLIP
IC1001A	2P00775	IC RADIATOR
Q1002A	1P01115	RADIATOR
R1020A	L3002	PIPE CORE
R1020B	L3002	PIPE CORE
R1021A	L3002	PIPE CORE
R1021B	L3002	PIPE CORE

(OUT OF CIRCUIT BOARDS)

MISCELLANEOUS		
A901	TC0007E	RF-VIDEO MODULATOR
KMNST-18	E3334	TERMINAL SOCKET
KMNSI-2	E4681	HOUSING, 9P
KMOS	E3329	CONNECTOR, 4P SOCKET
KMOST-4	E3325	CONNECTOR, TERMINAL SOCKET
KMSS	E4675	HOUSING, 3P
KMSSI	E3334	TERMINAL SOCKET
KMSS3	E3334	TERMINAL SOCKET
KMTS	E4685	HOUSING, 2PIN
KMTST-2	E3334	TERMINAL SOCKET
SW901	ES0146	KEYBOARD ASSEMBLY
SW902	ES0055	SWITCH, CARTRIDGE RESET
⚠ SW903	ES0083	SWITCH, POWER
⚠ W901	EW0102A	POWER CORD
W902	J012KGE	GROUND LEAD WITH TERMINAL
W903	J012KGE	GROUND LEAD WITH TERMINAL

7. CIRCUIT DESCRIPTION

The circuit of this machine consists of a CPU, MSX ROM, main RAM, VDP, PSG, PPI, VRAM as well as address bus, data bus and cartridge bus which are used to connect the foregoing devices.

7-1 BLOCK DIAGRAM

*MSX BASIC ROM is packaged as an internal storage in slot 0.

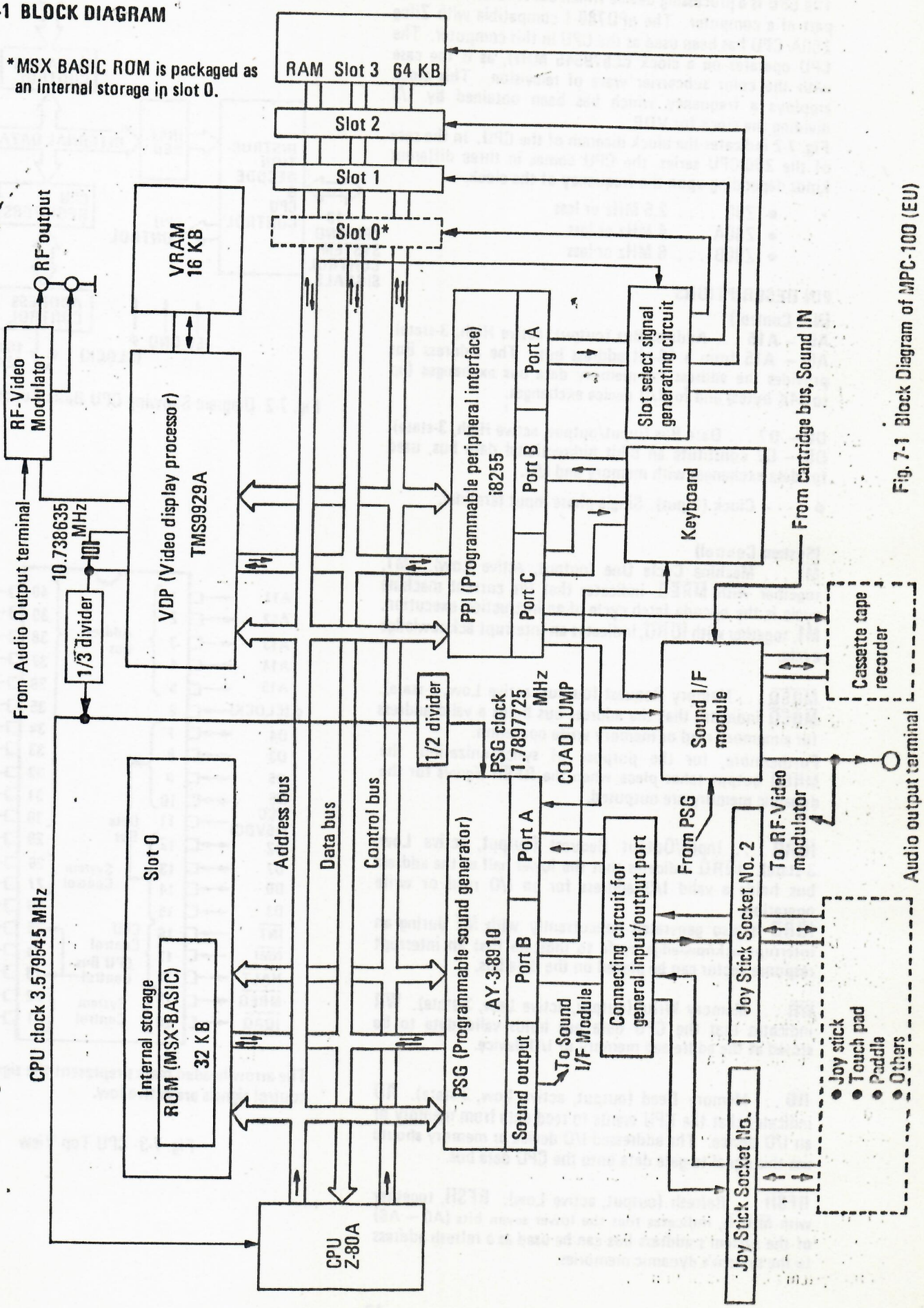


Fig. 7-1 Block Diagram of MPC-10D (EU)

2. CPU (Central Processing Unit)

The CPU is a processing device which constitutes the central part of a computer. The μPD780-1 compatible with Zilog Z80A CPU has been used as the CPU in this computer. The CPU operates on a clock (3.579545 MHz), as is the case with the color subcarrier wave of television. This clock employs a frequency which has been obtained by 1/3 dividing the clock for VDP.
Fig. 7-2 indicates the block diagram of the CPU. In the case of the Z80-CPU series, the CPU comes in three different kinds depending upon the frequency of the clock.

- Z80 . . . . 2.5 MHz or less
- Z80A . . . 4 MHz or less
- Z80B . . . 6 MHz or less

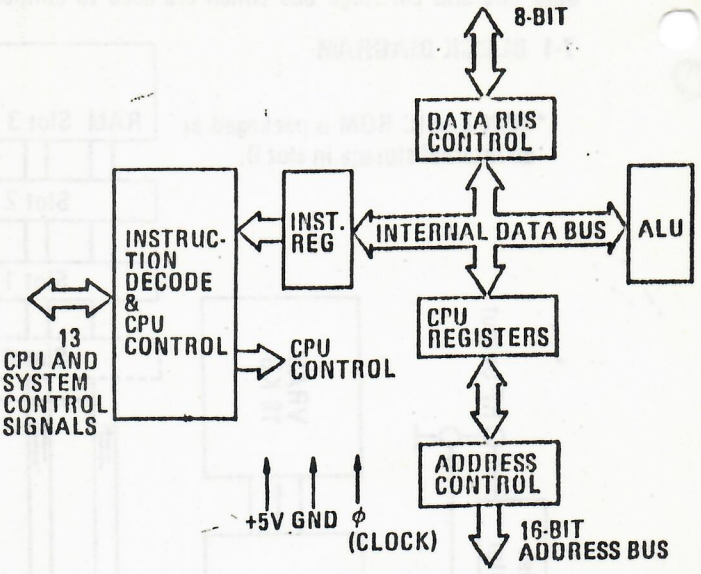


Fig. 7-2 Diagram Showing CPU Basic Functions

PIN DESCRIPTIONS

(Not Control)

A0 – A15 . . . Address Bus (output, active High, 3-state). A0 – A15 form a 16-bit address bus. The Address Bus provides the address for memory data bus exchanges (up to 64K bytes) and for I/O device exchanges.

D0 – D7 . . . Data Bus (input/output, active High, 3-state). D0 – D7 constitute an 8-bit bidirectional data bus, used for data exchanges with memory and I/O.

φ . . . . Clock (Input). Single-phase input terminal.

(System Control)

$\overline{M1}$ . . . Machine Cycle One (output, active Low). $\overline{M1}$, together with $\overline{MREQ}$, indicates that the current machine cycle is the opcode fetch cycle of an instruction execution. $\overline{M1}$, together with $\overline{IORQ}$, indicates an interrupt acknowledge cycle.

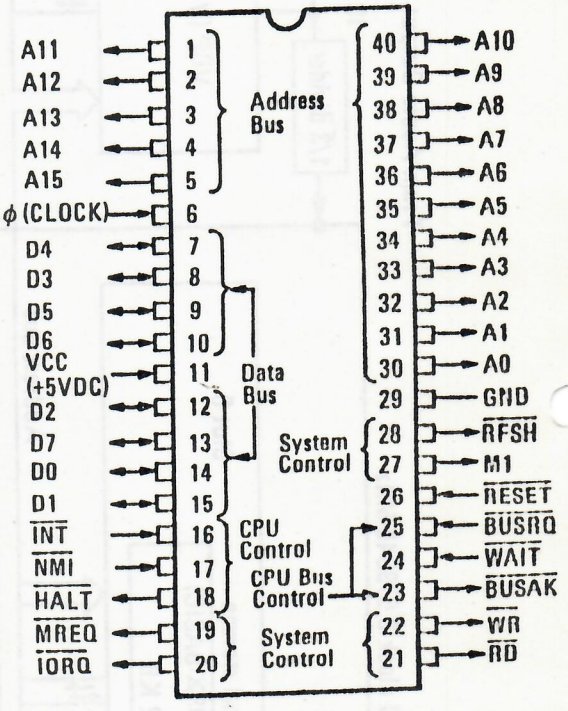
$\overline{MREQ}$ . . . Memory Request (output, active Low, 3-state). $\overline{MREQ}$ indicates that the address bus holds a valid address for a memory read or memory write operation.
Furthermore, for the purpose of synchronization, the $\overline{MREQ}$ output takes place when the $\overline{RFSH}$ signals for the dynamic memory are outputed.

$\overline{IORQ}$ . . . Input/Output Request (output, active Low, 3-state). $\overline{IORQ}$ indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation.
$\overline{IORQ}$ is also generated concurrently with $\overline{M1}$ during an interrupt acknowledge cycle to indicate that an interrupt response vector can be placed on the data bus.

$\overline{WR}$ . . . Memory Write (output, active Low, 3-state). $\overline{WR}$ indicates that the CPU data bus holds valid data to be stored at the addressed memory or I/O device.

$\overline{RD}$ . . . Memory Read (output, active Low, 3-state). $\overline{RD}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

$\overline{RFSH}$ . . . Refresh (output, active Low). $\overline{RFSH}$, together with $\overline{MREQ}$, indicates that the lower seven bits (A0 ~ A6) of the system's address bus can be used as a refresh address to the system's dynamic memories.



The arrow-headed marks represent the signal directions. Al control signals are active low.

Fig. 7-3 CPU Top View

Pin Descriptions (continued)

$\overline{HALT}$ . . . Halt State (output, active Low).
This is not used in the MSX system.

(CPU Control)
$\overline{INT}$ . . . Interrupt Request (input, active Low). Interrupt Request is generated by I/O devices. The CPU honors a request at the end of the current instruction if the internal software-controlled interrupt enable flip-flop (IFF) is enabled. $\overline{INT}$ is normally wire-ORed and requires an external pullup for these applications.

$\overline{WAIT}$ . . . Wait (input, active Low). $\overline{WAIT}$ indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter a Wait state as long as this signal is active. Therefore, the use of this signal makes it possible to use even low-speed I/O devices by synchronizing them with the CPU. Extended $\overline{WAIT}$ periods can prevent the CPU from refreshing dynamic memory properly.

$\overline{RESET}$ . . . Reset (input, active Low). $\overline{RESET}$ initializes the CPU as follows: it resets the interrupt enable flip-flop, clears the Program Counter and Registers I and R, and sets the interrupt status to Mode 0. During reset time, the address and data bus go to a high-impedance state, and all control output signals go to the inactive state. Note that $\overline{RESET}$ must be active for a minimum of three full clock cycles before the reset operation is complete.

$\overline{NMI}$ . . . Non-Maskable Interrupt (input, active Low). The $\overline{NMI}$ has a higher priority than $\overline{INT}$. This is not used in the MSX system.

(CPU Buss Control)
$\overline{BUSREQ}$ . . . Bus Request (input, active Low). Bus Request has a higher priority than NMI and is always recognized at the end of the current machine cycle. $\overline{BUSREQ}$ forces the CPU address bus, data bus, and control signals $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$ to go to a high-impedance state so that other devices can control these lines. $\overline{BUSREQ}$ is normally wire-ORed and requires an external pullup for these applications.

$\overline{BUSACK}$ . . . Bus Acknowledge (output, active Low). Bus Acknowledge indicates to the requesting device that the CPU address bus, data bus, and control signals $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$ have entered their high-impedance states. The external circuitry can now control these lines.

CPU TIMING
The Z80 CPU executes instructions by proceeding through a specific sequence of operations:
- Memory read or write
- I/O device read or write
- Interrupt acknowledge

The basic clock period is referred to as a T time or cycle, and three or more T cycles make up a machine cycle (M1, M2 or M3 for instance). Machine cycles can be extended either by the CPU automatically inserting one or more Wait states or by the insertion of one or more Wait states by the user.
For the detailed timing of the machine cycle and T time, consult speciality manuals regarding the CPU.

3. MEMORY

3-1 SLOT

To increase controllable memory capacity, the MSX has employed a method called "slot selecting." Unlike the hitherto-marketed computers in which memory devices are operated by hardware called "bank switching," memory devices are operated by software in the "slot selecting" method.
The MSX system is capable of operating four slots (0 through 3) normally. Moreover, it is possible to expand this system up to 16 slots. Here, one slot refers to a 64 KB address space.
As is evident from Fig. 7-5, each slot exists in the same address. Hence, signals may collide to each other without some countermeasures. In the MSX system, slots are selected through "slot selecting signals."

NOTE: The slot refers to a concept representing an address space. To distinguish from slots used as terminals whereby users connect memory devices, here the terminals are referred to as cartridge slots. Besides address bus and data bus, various control signals, +5 V DC and so forth are connected to the cartridge bus. It is, therefore, possible to connect not only memory devices but also I/O devices (e.g. light pen unit) to the cartridge slot.

On the CPU of the MSX system, 64 KB memory is operated by slot select signals and 16-bit address. Furthermore, this 64 KB memory space is controlled after it has been divided into four divisions, thus forming 16 KB memory spaces (called "page"). Any slot can be assigned to each page, thereby constituting a piece of software.
Fig. 7-7 indicates the slot configuration of this machine. The machine has been so designed that slots 1 and 2 are used as cartridge slots to which peripheral devices can be connected. The MSX-BASIC interpreter has been assigned to pages 0 and 1 of slot 0, whereas the 64 KB RAM has been assigned to slot 3.

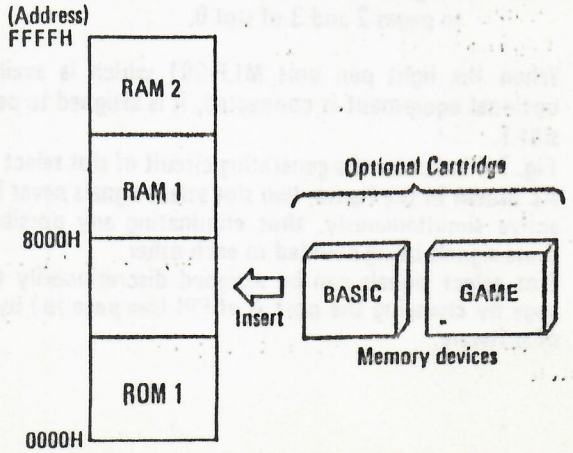


Fig. 7-4 Example of Bank Switching

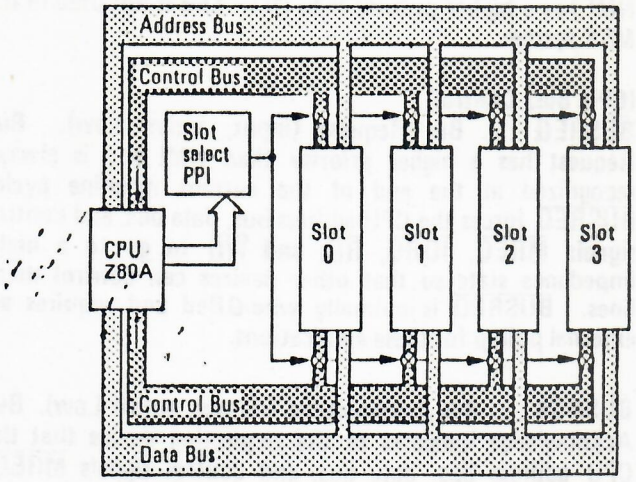


Fig. 7-5 Schematic Diagram of Slot Selecting

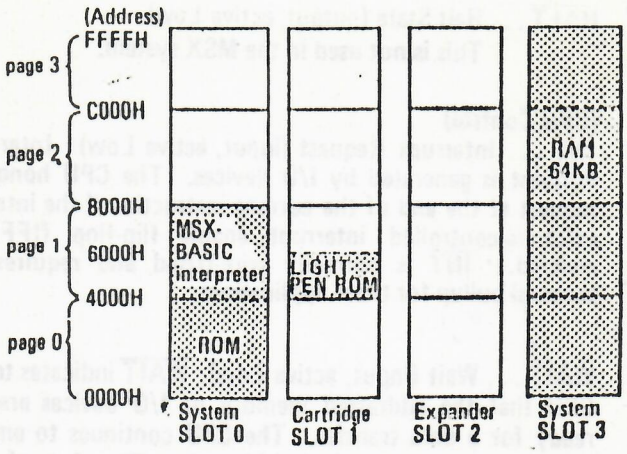


Fig. 7-6 Memory Map of Machine

Page No.	Control Address	Address	
		A14	A15
0	0000H ~ 3FFFH	0	0
1	4000H ~ 7FFFH	1	0
2	8000H ~ BFFFH	0	1
3	C000H ~ FFFFH	1	1

Table. 7-1 Page and Address

NOTE: Although the preceding paragraph says that any software can be assigned to each page, in actual application, there are the following requirements for the MSX system.

- The MSX-BASIC interpreter should be assigned to pages 0 and 1 of slot 0.
- When the system is started, there should be RAM of not less than 8 KB in any slot in the direction of lower order from FFFFH.
- When the MSX-DOS (Optional System Soft) is used, there should be 64 KB RAM contiguously in one slot.

In accordance with the above-described requirements, in this machine, 64 KB RAM has been assigned to slot 3, while no device has been assigned to pages 2 and 3 of slot 0.

When the light pen unit MI.P-001 which is available as optional equipment is connected, it is assigned to page 1 of slot 1.

Fig. 7-7 indicates the generating circuit of slot select signals. As shown in the figure, two slot select signals never become active simultaneously, thus eliminating any possibility of these signals being collided to each other.

Slot select signals can be assigned discretionarily to each page by changing the port A of PPI (see page 20) by means of software.

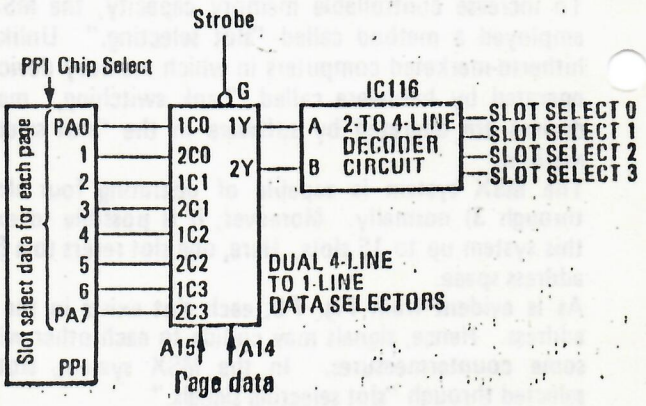


Fig. 7-7 Generating circuit of Slot select signals

3-2 MSX ROM

As shown in Fig. 7-6, a 32 KB ROM of the MSX-BASIC interpreter exists in slot 0. This is a 262,144-bit mask ROM which memorizes programs equivalent to approximately 32 KB.

Fig. 7-9 indicates the block diagram of the ROM, whereas Table 7-2 shows the functions of the terminals.

Furthermore, the following indicates the procedure whereby data are read from the ROM.

1. The CPU outputs signals of the address to be read (address data) to the address bus.
2. The $\overline{CS}$ of the ROM becomes effective (low-level). (Normally, this terminal functions as a chip selector.)
3. Data (programs) are outputed to the data bus. Then, the data are inputted by the CPU.

A0 – A14	Address input: The CPU has terminals of A0 through A15 in order that memory up to 64 KB may be controlled. However, the ROM has terminals of A0 through A14 only, for this ROM has a capacity of 32 KB.
D0 – D7	Data output: Output of data contained in the ROM
$\overline{OE}$	Output enable input: Selection as to whether output is produced or not
$\overline{CS}$	Chip enable input: Timing signal of data output
VDD	Power supply terminal: Used at +5V

Table. 7-2 Pin Descriptions of ROM

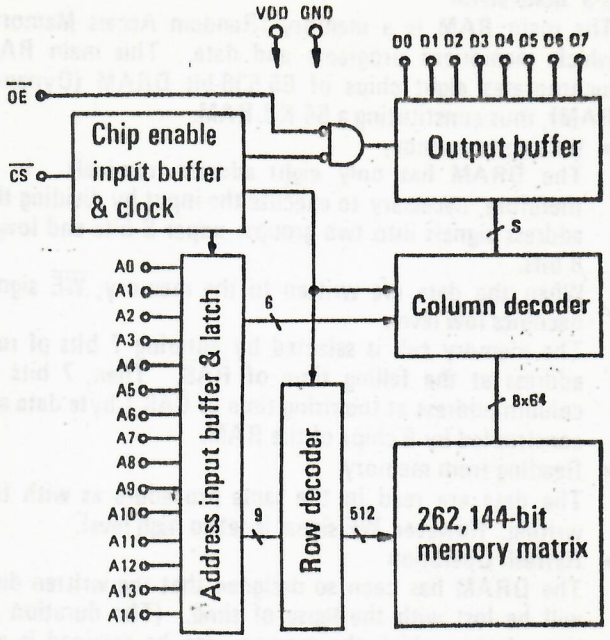


Fig. 7-8 Block Diagram of ROM

INPUT "1" LEVEL	2.2 ~ Vcc	(V)
INPUT "0" LEVEL	−0.3 ~ 0.8	(V)
OUTPUT "1" LEVEL	4.4	(V)
OUTPUT "0" LEVEL	0.4	(V)

Vcc = 5V ± 10%
Vss = 0V

Table. 7-3 Signal specification

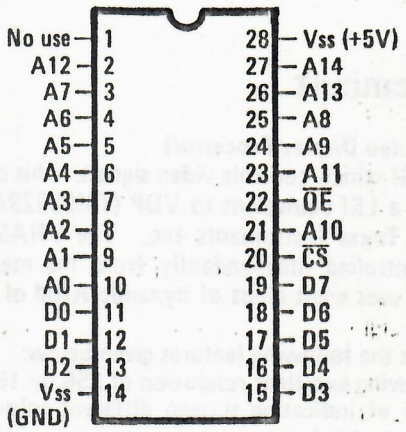
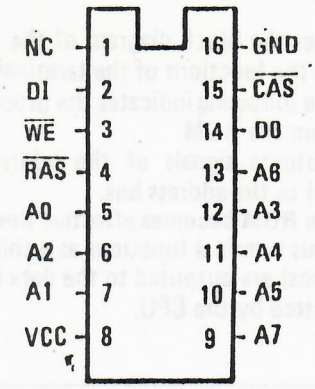


Fig. 7-9 ROM terminals

3-3 Main RAM

The main RAM is a memory (Random Access Memory) which memorizes programs and data. This main RAM incorporates eight chips of 65,536-bit DRAM (Dynamic RAM), thus constituting a 64 KB RAM.

- Writing to memory
  The DRAM has only eight address terminals. It is, therefore, necessary to execute the input by dividing the address signals into two groups: upper 8 bits and lower 8 bits.
  When the data are written to the memory, $\overline{WE}$ signal becomes low level.
  The memory cell is selected by entering 7 bits of row address at the falling time of $\overline{RAS}$. Then, 7 bits of column address at the rising time of $\overline{CAS}$ 1 byte data are constructed by 8 chips of the RAM.
- Reading from memory
  The data are read in the same procedure as with the writing. However, $\overline{WE}$ signal is set to high level.
- Refresh Operation
  The DRAM has been so designed that the written data will be lost with the lapse of time. (The duration of time during which the memory can be retained is approximately 2 ms.) Hence, the CPU constantly carries out the operation called "refresh" so that the DRAM may retain its memory. This operation takes place simultaneously on eight chips of the DRAM by providing the address terminals of the DRAM with "refresh address" (A0 through A6) and $\overline{RAS}$ signals before the duration of 2 ms during which the memory is retained expires.
  Furthermore, the refresh addresses are independent from the program counter (PC) located inside the CPU.
  Consequently, the refresh operation can be carried out while the CPU is reading programs from the memory or is decoding instructions.



VDD: +12V power supply
VCC: +5V power supply
VBB: −5V power supply
DI: Data input
DO: Data output
WE: Writing signal
CAS and RAS: Strobe signals of address

Fig. 7-10 RAM Terminals

4. VIDEO CIRCUIT

4-1 VDP (Video Display Processor)

This is an LSI which controls video signals. This computer incorporates a LSI equivalent to VDP (TMS9929A) manufactured by Texas Instruments Inc. The VRAM (Video RAM) is controlled independently from the main RAM. (The VRAM uses eight chips of dynamic RAM of 16K bits x 1 bit.)

This VDP has the following features given below:

- Display having excellent resolution of 256 by 192 dots
- Capability of indicating sixteen different colors including transparent color
- Split function which is very handy in producing superimposed images and animation
- Output of color distinction signals of R-Y, B-Y and Y
- Output of timer interruption pulses at intervals of 1/50 second
  (INT terminal of the CPU)

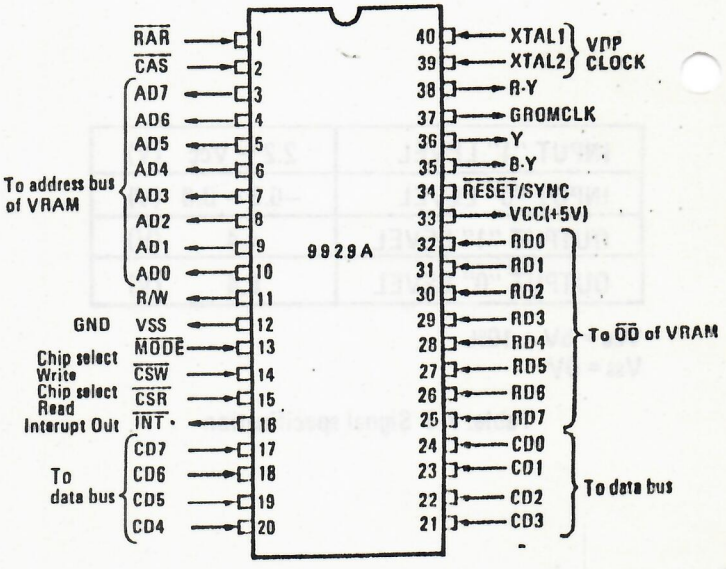


Fig. 7-11 indicate the terminal nomenclature of the VDP.

Addresses of 98H and 99H have been assigned as the I/O port of the VDP. A0 is connected to MODE. When the 98H is selected, "writing/reading data bytes to/from VRAM" takes place. Also, when the 99H is selected, "writing to one of the eight VDP write-only registers or reading the VDP Status Register" takes place.
VDPCS (VDP Chip Select) is obtained by A3, A4 and A5. $\overline{CSW}$ and $\overline{CSR}$ are inverted NAND output of VDPCS/$\overline{WR}$ combination and VDPCS/$\overline{RD}$ combination respectively.
VDPCS becomes L level when the address set by the CPU is 98H or 99H, indicating the state of input/output to the VDP. (Actually, VDPCS becomes L level when the address set by the CPU is one of those 98H through 9FH.)

PIN DESCRIPTIONS (VDP Control)

$\overline{MODE}$: ..... CPU interface mode select input (active low.) It determines whether the CPU is to control the VDP or VRAM by means of the address A0.
(When A0 is in L level, the CPU controls the VRAM.)

$\overline{CSW}$: ..... CPU-VDP write strobe input (active low.) When it is active, the eight bits on CD0 ~ CD7 are strobed into the VDP.

$\overline{CSR}$: ..... CPU-VDP read strobe input (active low.)

CD0 ~ CD7: .. CPU data bus input/output. CD0 is the most significant bit.

$\overline{XTAL1}$, ... 10.7 MHz Crystal inputs. VDP is controlled
XTAL2: by this basic clock. When driven externally, both inputs must be driven.

$\overline{RESET}$/SYNC: Reset and external Sync. inputs. This pin is a trilevel input pin. When it is below 0.8 volts, $\overline{RESET}$ initializes the VDP. When it is above 9 volts, $\overline{RESET}$ is the synchronizing input for external video.

B-Y: ..... B-Y color difference output.

R-Y: ..... R-Y color difference output.

Y: ..... Y signal output.

$\overline{RESET}$/SYNC inputs the reset signal for the VDP and the synchronization signal by which the video signals (R-Y, B-Y, Y) are externally synchronized. (Only $\overline{RESET}$ input, for this machine employs internal synchronization). Using the basic clock from the XTAL terminal, the VDP can produce the R-Y and B-Y signals as well as the Y signal which contains its own horizontal and vertical synchronization signals.

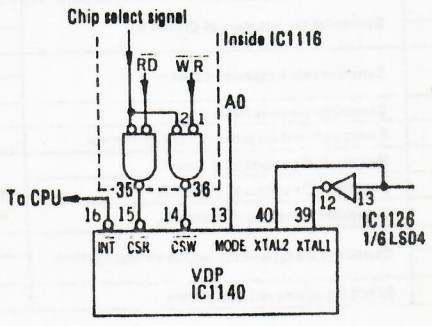


Fig. 7-12 VDPCS Circuit

(VRAM Control)

$\overline{RAS}$: ..... VRAM row address strobe output (active low.)

$\overline{CAS}$: ..... VRAM column address strobe output (active low.)

AD0 ~ AD7: .. VRAM address/data bus output. This bus line is for multiplexed high and low order VRAM address and for the output data bytes. A0 is the most significant bit and is used only for data and not for addressing. Care must be exercised in assuring proper orientation of the 9929A address outputs to the VRAM address inputs.

R/W: ..... VRAM write strobe output (active low.)

RD0 ~ RD7: .. VRAM read data bus input. RD0 is the most significant bit.

GROMCLK: .. VDP output clock output. Clock employs a frequency 1/24 of that of the XTAL clock.

$\overline{INT}$: ..... CPU interrupt output (active low.) The VDP $\overline{INT}$ output pin is used to generate an interrupt at the end of each active-display scan, which is about every 1/50 second.

4-2 VRAM (Video Random Access Memory)

VRAM refers to dynamic RAMs that are connected to the VDP and it is independent from the system bus.
The VRAM employs eight chips of a dynamic RAM of 16K-bit x 1 bit.

4-3 RF-VIDEO MODULATOR

The picture on the television set is composed of the synchronization signals such as horizontal synchronization signal, vertical synchronization signal and color burst signal, and syncronizing serial data. This RF-Video Modulator can generate these signals.

This module converts the Y, R-Y, B-Y signals which are outputed from the VDP to composite video signal and RF signal (UHF 36 CH). The equalizer in the module performs phase compensation in the high frequency region of the Y signal. The VCO circuit having X1 and IC1 produces subcarrier of 4.43 MHz.

The table below describes color signals of the VDP inputted to this module. (Specified value)

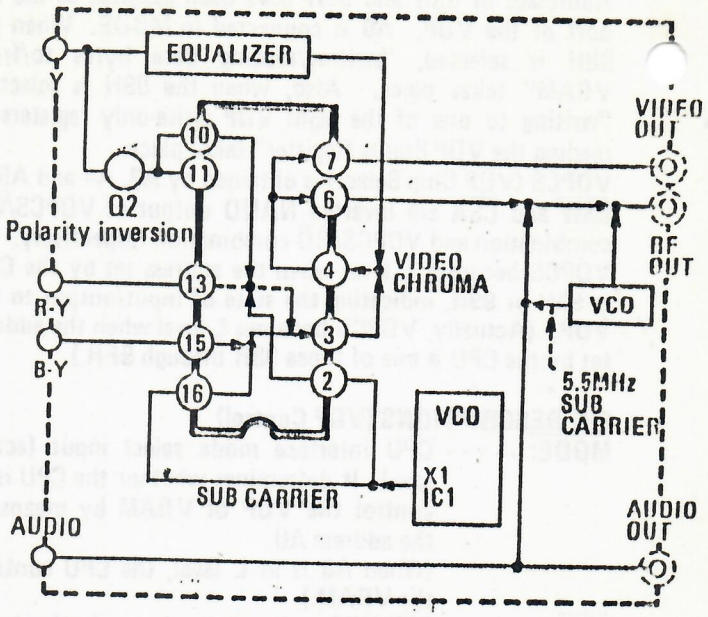


Fig. 7-13 RF-VIDEO Modulator Block Diagram

Color No.	1	2	3	4	5	6	7	8	9	10	11	12
Color	Black	Green	Light Green	Dark Blue	Light Blue	Dark Red	Syan	Red	Light Red	Dark Yellow	Light Yellow	Dark Green
Y signal (V)	0	0.36	0.46	0.27	0.36	0.32	0.5	0.36	0.46	0.5	0.55	0.32
R-Y signal (V)	0	−0.3	−0.23	−0.05	−0.03	0.27	−0.35	0.35	0.35	0.08	0.08	−0.26
B-Y signal (V)	0	−0.2	−0.15	0.4	0.35	−0.13	0.17	−0.15	−0.15	−0.3	−0.23	−0.18

Color No.	13	14	15	–	–
Color	Mazen tor	Gray	White	Color Burst	Sync
Y signal (V)	0.36	0.55	0.68	0	−0.32
R-Y signal (V)	0.2	0	0	0.2	0
B-Y signal (V)	0.15	0	0	−0.28	0

Table. 7-4 Color signals of the VDP

5. PSG (Programmable Sound Generator)

This is an LSI which synthesizes sound signals. This LSI is equivalent to PSG (AY-3-8910) manufactured by General Instruments. Corp. This PSG has following functions.

- The PSG has a tone generator having three channels (A, B and C) and a noise generator, thereby making it possible to produce triple chord performance and artificial sounds used in games, etc.
- The PSG has two general 8-bit input/output ports (joy stick terminal), to which tablet and touch pad, etc., besides joy stick, can be connected.
- The PSG can read signals from a cassette tape recorder.

Since all functions of the PSG are controlled by the host processor via a series of register loads, a detailed description of the PSG operation can best be accomplished by relating each PSG function to the control of its corresponding register.

Register No.	Function	Data range
0	Determines the frequency of channel A.	0 – 255
1		0 – 15
2	Determines the frequency of channel B.	0 – 255
3		0 – 15
4	Determines the frequency of channel C.	0 – 255
5		0 – 15
6	Determines the noise frequency.	0 – 31
7	Selects a channel for tone and noise generation.	0 – 63
8	Determines the volume of channel A.	0 – 15 Volume variation occurs when 16 is selected.
9	Determines the volume of channel B.	
10	Determines the volume of channel C.	
11	Determines the cycle of the volume variation pattern.	0 – 255
12		0 – 255
13	Selects the volume variation pattern.	0 – 14

Table. 7-5 PSG register functions and the write data range

PIN DESCRIPTIONS

DA0 ~ DA7: · · Data/Address 0 ~ 7 input/output/high impedance 8 bit bidirectional bus. This 8-line bus is used when the CPU send datas or addresses to the PSG or when the CPU receive datas from the PSG. In the addresses mode, the pins DA0 through DA3 refer to the registers #0 through #15. In data mode, the pins DA0 through DA7 correspond to each bit of the register.

A8, $\overline{A9}$: · · · · · Address 8, Address 9 input. This is used when the PSG is used as the chip select of the memory.

$\overline{RESET}$: · · · · · Reset input (active low.) At the time of initialization or when the power is turned ON, all registers are reset to "0" by setting this pin to logical "0".

CLOCK: · · · · PSG CLK TTL compatible input. The CPU CLK is 1/2 divided and added as the timing standard of the tone, noise and envelope. (The 1/2 dividing is performed at the IC116 GATE ARRAY.)

BDIR, BC1, 2: Bus Direction, Bus Control 1, 2 input. The PSG functions are set as indicated below. The BC2 is pulled up to +5V. The BDIR and BC1 are obtained by decoding control signals of the CPU at IC1116.

BDIR	BC1	BC2	Function
0	0	1	IN ACTIVE
0	1	1	READ FROM PSG
1	0	1	WRITE TO PSG
1	1	1	LATCH ADDRESS (Select register)

ANALOG CHANNEL A, B, C: · · · Sound wave form output (1Vp-p signal: max.) Complicated sound wave forms are outputed through the D/A converter.

IOA0 ~ IOA7, IOB0 ~ IOB7: 8 bit Data input/output. When peripheral devices are connected through the Joy Stick Terminals to IOA or IOB of PSG, 8-bit data can be inputed/outputed from the PSG to the peripheral devices or from the external devices to the PSG. Since each terminal incorporates a pull-up resistor, it becomes active low under the input mode.

TEST1, 2: · · · · Outgoing test terminal. These terminals are for manufacturer use only and should be left open.

NOTE: On the MSX system, the pin functions of the IOA and IOB have been determined as follows:
IOA6: Matrix specification of the keyboard.
IOA7: Signal input from a cassette tape.
IOB6: Selection of the input (joy stick 1 or 2) of the port A.

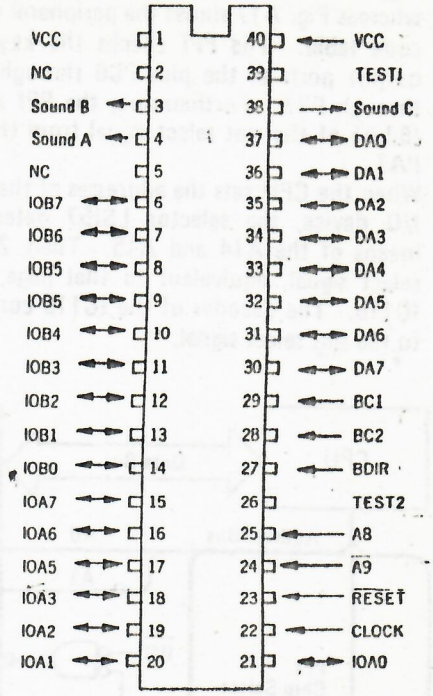


Fig. 7-14 Terminal Nomenclature of PSG

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6. PPI (Programmable Peripheral Interface)

This LSI has three sets of 8-bit input/output port. This can be used for data input/output, status signal input and control signal output, which are controlled by CPU by means of software, etc. Fig. 7-15 shows the terminal nomenclature of the LSI.

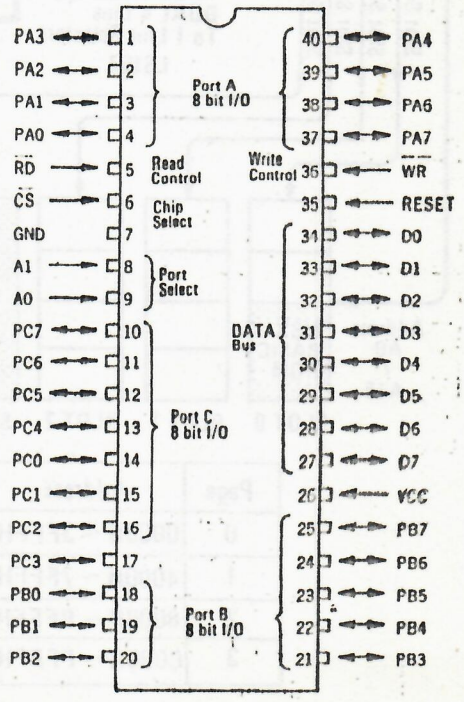


Fig. 7-15 Terminal Nomenclature of PPI

Fig. 7-16 shows the internal block diagram of the PPI, whereas Fig. 7-17 shows the peripheral circuit and character code table. The PPI checks the key input using input/output ports at the pins PC0 through PC3 and pins PB0 through PB7. Furthermore, the PPI always outputs data (8-bit) of the slot select signal from the pins PA0 through PA7.

When the CPU sets the addresses of the memory device and I/O device, the selector LSI57 determines the page by means of the A14 and A15. Then, 2-bit data of the slot select signal, equivalent to that page, is outputed to the IC116. The decoder of the IC116 converts this 2-bit data to the slot select signal.

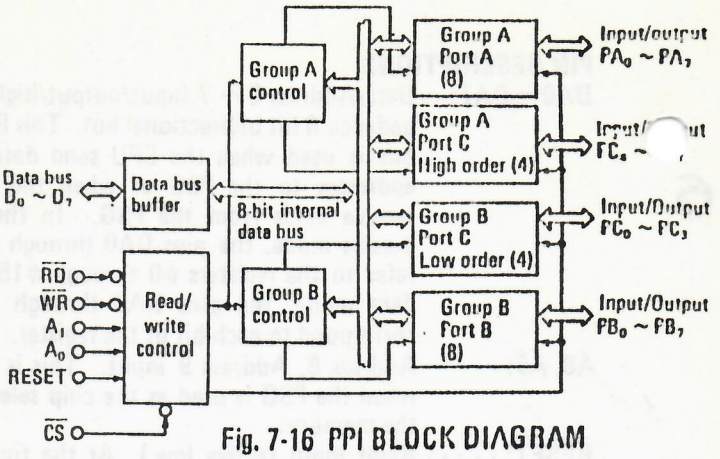
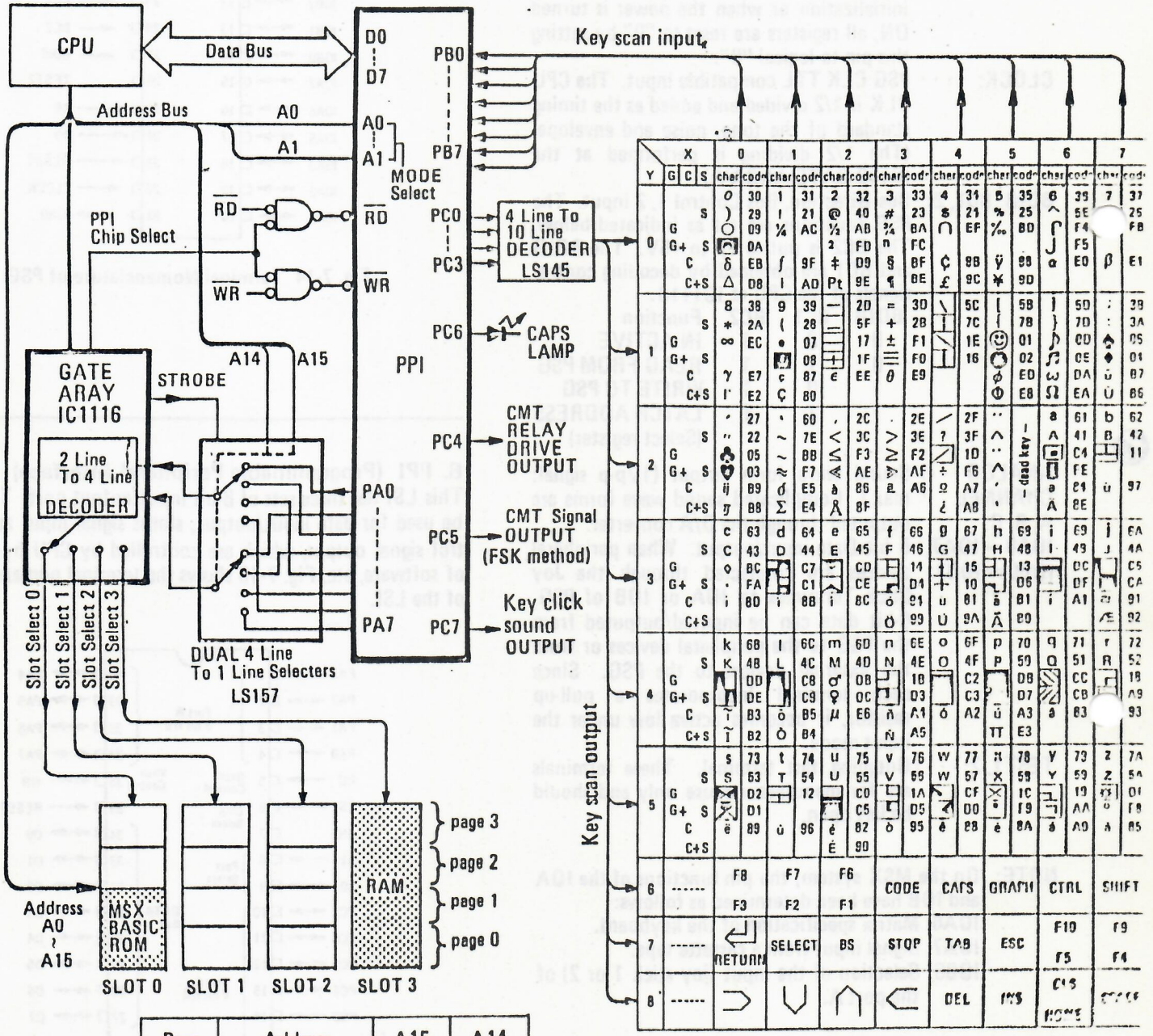


Fig. 7-16 PPI BLOCK DIAGRAM



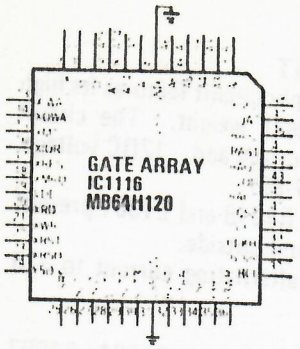
Page	Address	A15	A14
0	0000H ~ 3FFFH	0	0
1	4000H ~ 7FFFH	0	1
2	8000H ~ BFFFH	1	0
3	C000H ~ FFFFH	1	1

G: Key input while "GRAPH" key is being pressed.
C: Key input while "CODE" key is being pressed.
S: Key input while "SHIFT" key is being pressed.

Fig. 7-17 PPI Peripheral Circuit and Character Code Table

7. GATE ARRAY

This LSI produces various control signals and timing signals to be used in the MSX system.
The use of this LSI has contributed to simplification and improved performance of the logic circuits in the computer.



TOP VIEW

- C Mos LSI
- Flat Package 48 Pin
- Power supply 5V ± 0.25 VDC

Fig. 7-18 Schematic Diagram of Gate Array

Table. 7-6 PIN DESCRIPTION of GATE ARRAY

Pin No.	I/O	Name	Function
1	I	A0	Data creation
2	I	A3	CS (Chip Select) creation
3	I	A4	"
4	I	A5	"
5	I	A6	CS creation and address setting
6	–	VSS	GND
7	I	A7	CS creation and address setting
8	I	A14	Page Select (RAS 1, 2)
9	I	A15	CS1, 2 creation and data creation
10	I	D0	STRB creation
11	O	D1	BUSY output
12	I	CLK	CPU CLK input (3.58 MHz)
13	I	XIWA	TEST signal input
14	O	XOWA	TEST timing output
15	I	XM1	CPU Machine cycle 1 input
16	I	XIOR	CPU I/O Request input
17	I	XPFS	CPU Memory Refresh input
18	I	XMRQ	CPU Memory Request input
19	–	VDD	+5V
20	I	XRD	CPU Read timing input
21	I	XWR	CPU Write timing input
22	I	XRST	$\overline{\text{RESET}}$ input
23	O	XRSO	Slot select strobe output
24	O	Y50	PPI Chip Select output
25	O	CSR0	MSX ROM Chip Select
26	I	SL11	Slot Select bit 1 input
27	I	SL21	Slot Select bit 2 input
28	O	SLT1	Slot Select 1 output
29	O	SLT2	Slot Select 2 output
30	O	SLT3	Slot Select 3 output
31	–	VSS	GND
32	I	BUSY	Printer Busy input
33	O	STRB	Printer Strobe output
34	O	CSP	Printer Chip Select output
35	O	Y3RD	VDP $\overline{\text{RD}}$ output
36	O	Y3WR	VDP $\overline{\text{WR}}$ output
37	O	BC1	PSG BC1 output
38	O	BDIR	PSG BDIR output
39	O	CLKH	PSG CLK output (1.7 MHz)
40	O	CS1	Chip Select 1 (&H4000~&7FFF)
41	O	CS2	Chip Select 2 (&H8000~&BFFF)
42	O	RA01	
43	–	VDD	+5V
44	O	RA02	
45	O	RAS1	Memory $\overline{\text{RAS}}$ page 3 select
46	O	RAS2	Memory $\overline{\text{RAS}}$ page 2 select
47	O	OA7	Memory Address A7
48	O	XSEL	Memory Address selector

8. SOUND I/F MODULE

The PSG and the PPI are connected through this module to the Audio Output Terminal and Cassette Recorder Terminal.
This module performs impedance matching and signal mixing between the devices and terminals.

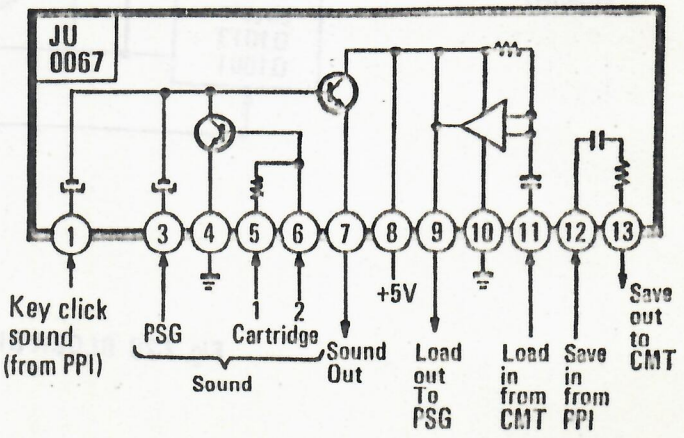


Fig. 7-19 Circuit diagram of SOUND I/F MODULE

). POWER SUPPLY CIRCUIT

A switching regulator power supply circuit features its high efficiency, compact size and light weight. The circuit produces +5DC voltage, +12DC voltage and –12DC voltage.

Circuit Operation (Refer to Fig. 7-20)

Those circuits of R1001, C1001, R1019 and L1001 prevent noise emitting from both inside and outside.

The D1001 and C1010 rectify alternating current to 310 DC V.

When powered, a DC voltage is, through D1001, R1002 impressed to the base of Q1002, which is forward-biased Q1002, and a small current flows into L1 of T1001. This generates voltage in L2 of T1001, and allows a base current to flow in the following sequence; L2 – the base of Q1002 – the emitter of Q1002 – R1007 – R1003 – D1002 and then L2, which increases collector current of Q1002 rapidly and linearly.

When the collector current reaches the saturation level, the current flowing through L1 becomes constant and the polarity of the voltage generated across L2 reverses because the magnetic flux in L1 is no longer changing. This causes the base current of Q1002 to decrease, thus making Q1002 non-conductive immediately.

Energy stored in L1 during the time when current is increasing (Q1002 is conductive) is transferred to coils L3, L4 and L5 when current is decreasing (Q1002 is non-conductive). After it has been rectified by diode (D1007, D1008, D1009) and electrolytic capacitor, it is supplied to the load.

When the energy in L1 is released to L3, L4 and L5, a pulse is generated in L2 in the reverse direction.

When this happens, Q1002 is forward-biased again, and the above processes are repeated, resulting in oscillation. (The oscillation frequency is about 25 KHz.)

Because of energy applied to the coils of L3, L4 and L5, DC power for appling to the load is rectified by a diode and electrolytic capacitor.

The D1009, C1014, C1015 and C1016 produce a voltage of +5V. This voltage also serves as a reference voltage for +12V and –12V. The D1008, R1021 and C1018 produce +16V AC, from which power supply of +12V ± 5% (500 mA max.) is obtained by the operation of the IC1001. The D1007 produces power supply of +8V using the R1020 and C1020. When thus-obtained +8V is applied to the IC1003 (+5V: GND), a voltage of –12V is outputed.

The variation in voltage at the pin R of the IC1002 corrects +5V as follows: As the voltage of the pin K of the IC1002 varies, the current of the D1013 changes; → As the bias voltage at the base of the Q1001 varies, the duty ratio of the ON/OFF time of the Q1001 changes; → As the duty ratio of the ON/OFF time of the Q1002 varies, the energy stored at the L1 changes; → The energy (+5V AC) generated at the L5 changes.

The shut down (Q1050, Q1051 and Q1053) suspends outputs of +5V, +12V and –12V when the cartridge is inserted to the cartridge slot.

Thereby, it prevents MOS IC in the cartridge from being damaged. When the cartridge is inserted completely, the outputs are produced again.

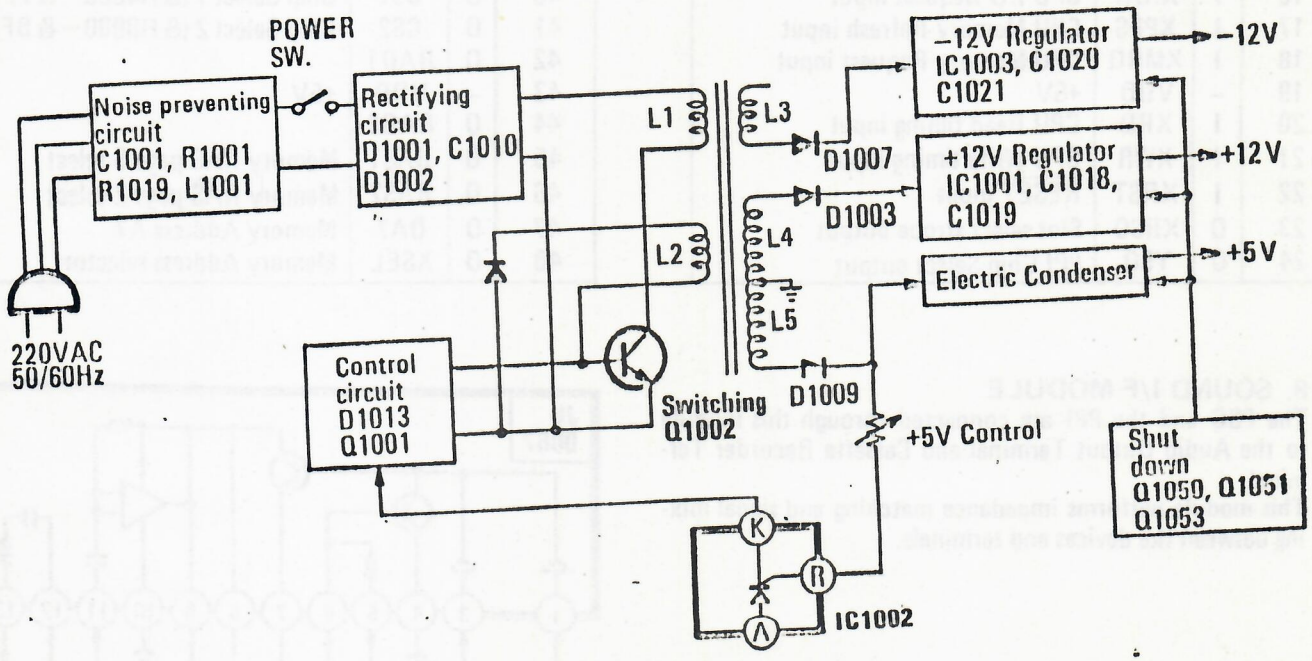
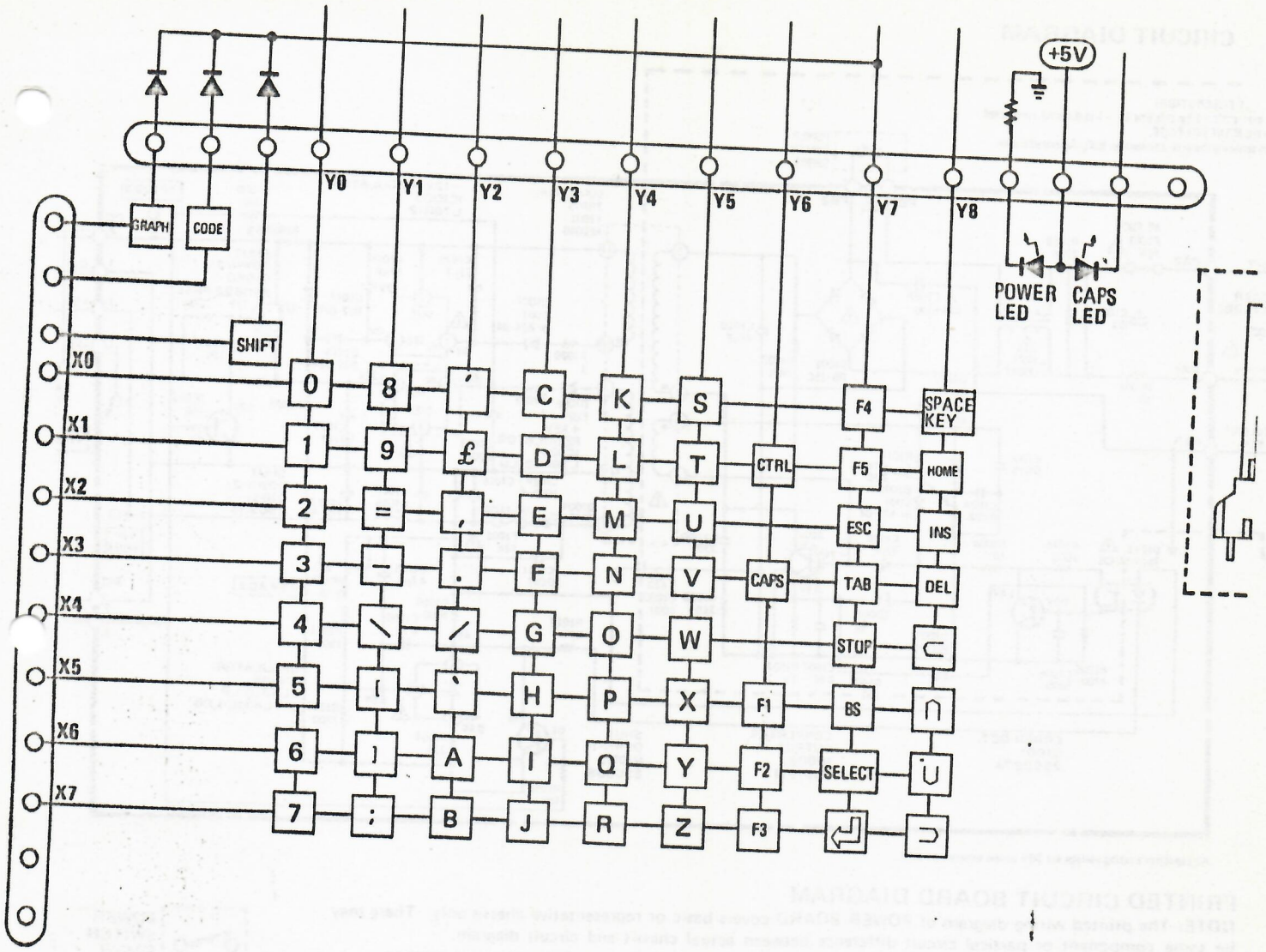
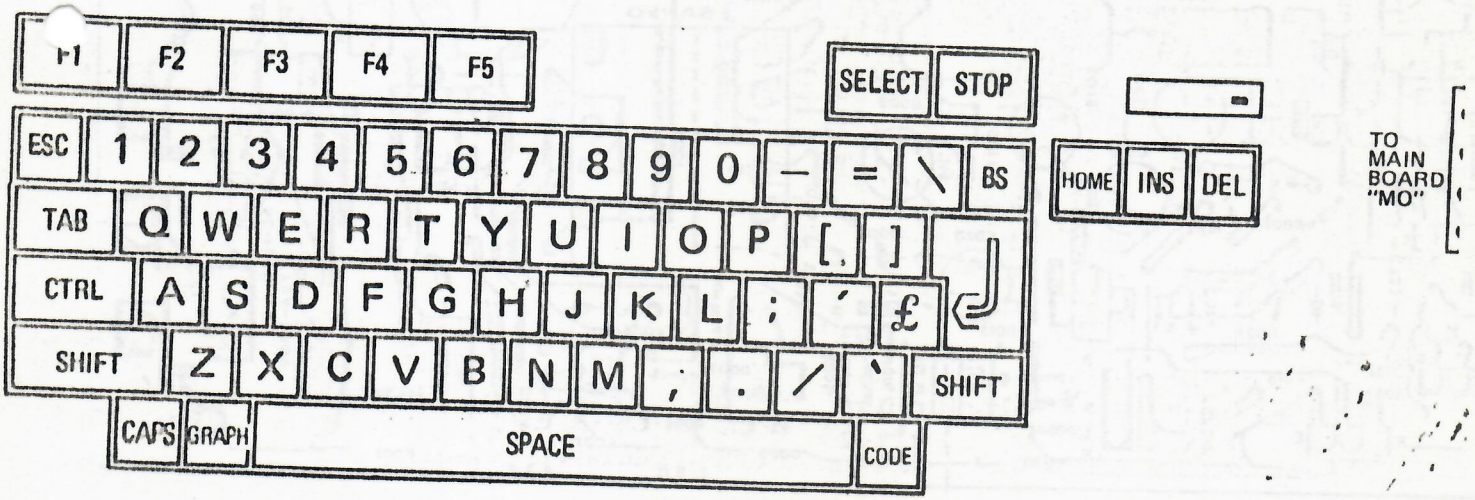


Fig. 7-20 BLOCK DIAGRAM of power supply circuit

8. SCHEMATIC DIAGRAMS

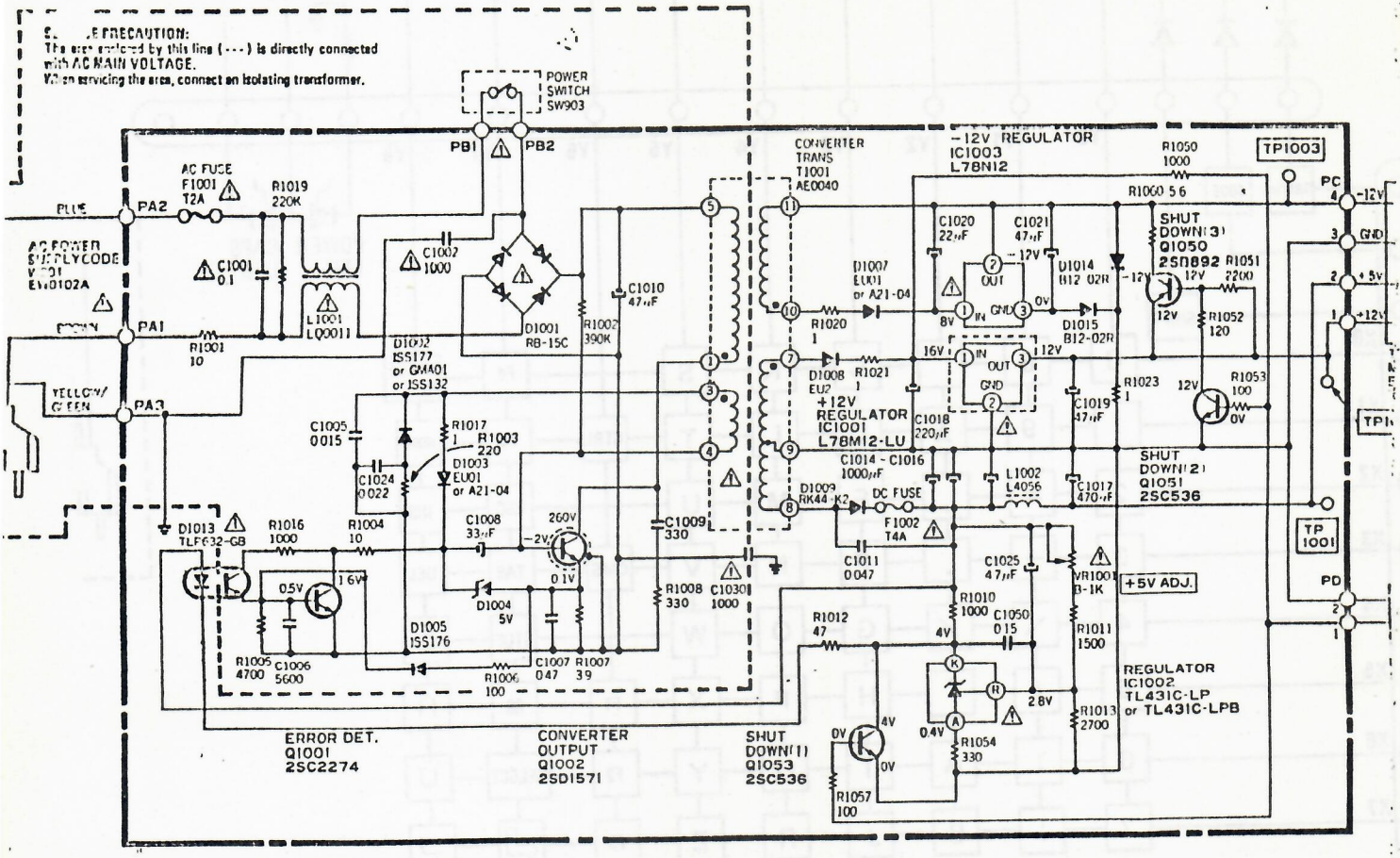
KEY BOARD CIRCUIT DIAGRAM





POWER BOARD

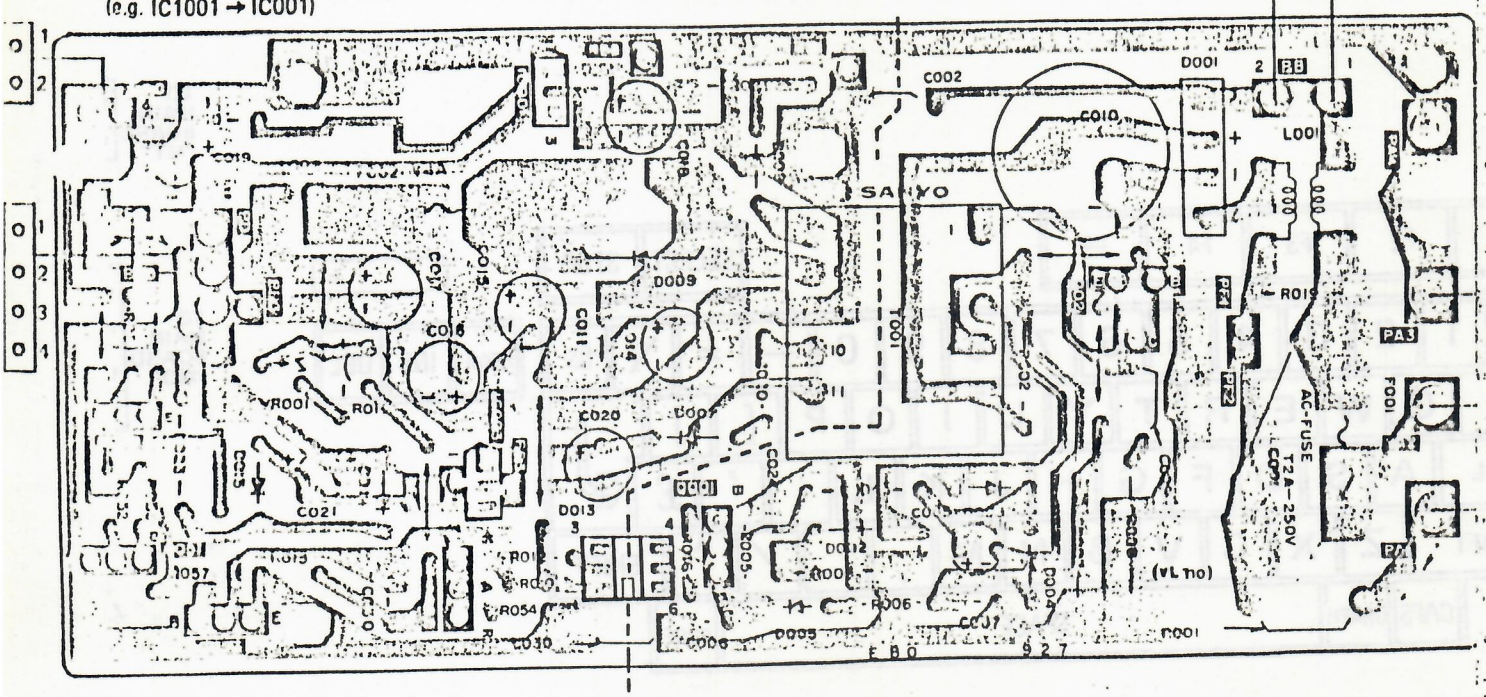
CIRCUIT DIAGRAM



All capacitor's rating voltage are 50V unless otherwise noted.

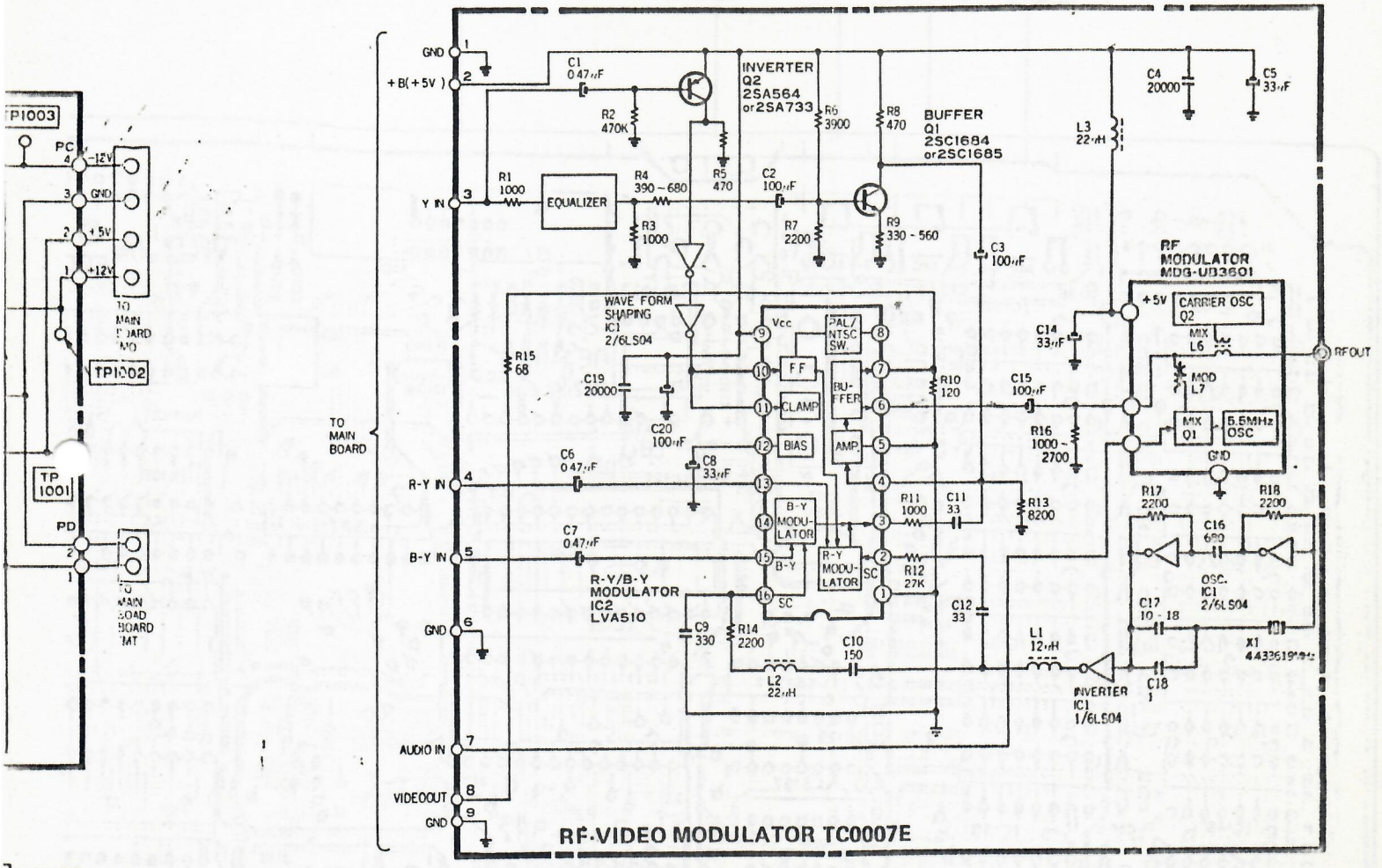
PRINTED CIRCUIT BOARD DIAGRAM

NOTE: The printed wiring diagram of POWER BOARD covers basic or representative chassis only. There may be some component or partical circuit difference between actual chassis and circuit diagram.
The location numbers of this printed circuit board indicate the last three figures of the schematic location.
(e.g. IC1001 → IC001)



RF•VIDEO MODULATOR

CIRCUIT DIAGRAM



RF-VIDEO MODULATOR TC0007E

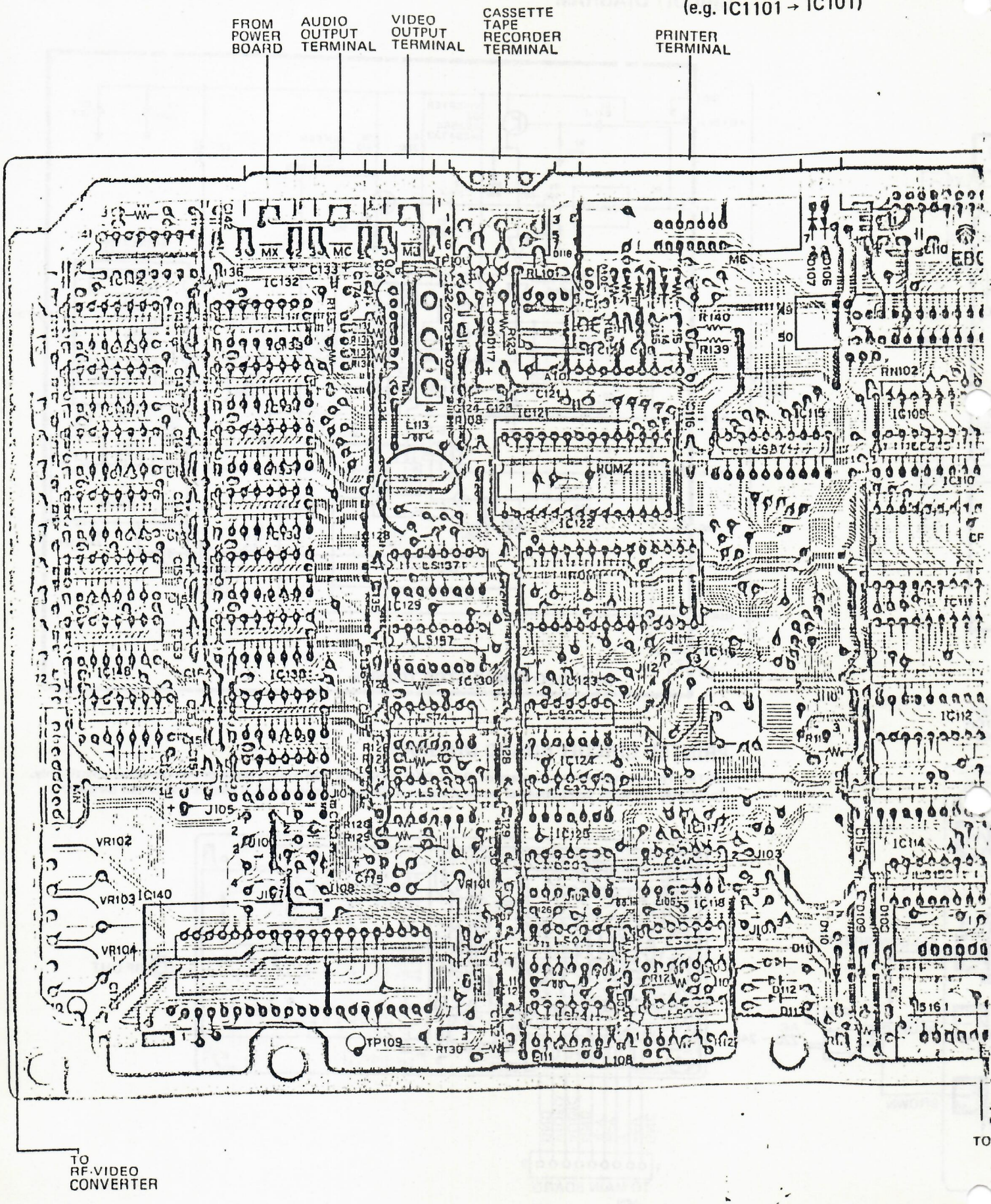
PRINTED CIRCUIT BOARD DIAGRAM

NOTE: The printed wiring diagram of RF-VIDEO MODULATOR covers basic or representative chassis only. There may be some component or partical circuit difference between actual chassis and circuit diagram.

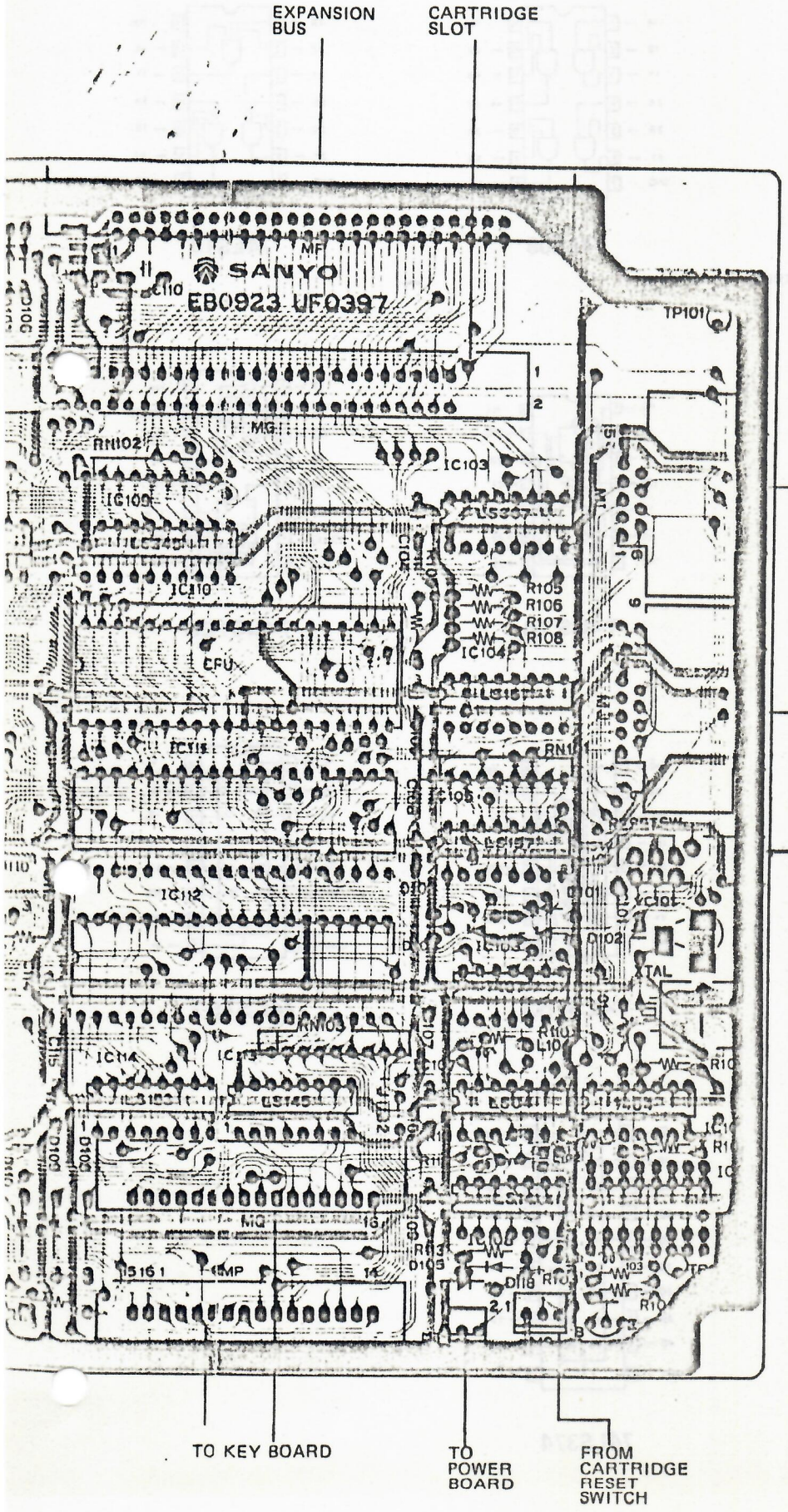
MAIN BOARD

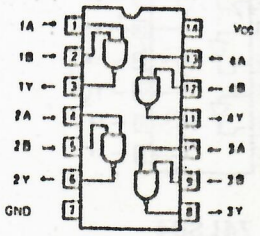
PRI :ED CIRCUIT BOARD DIAGRAM

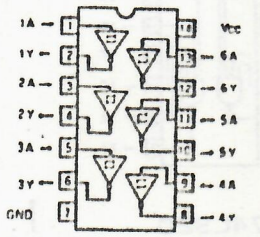
NOTE: The printed wiring diagram c
chassis only. There may be some cc
actual chassis and circuit diagram.
board indicate the last three figures o
(e.g. IC1101 → IC101)

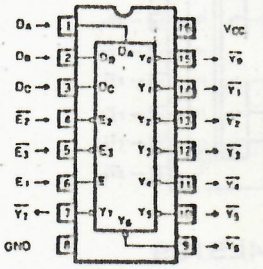


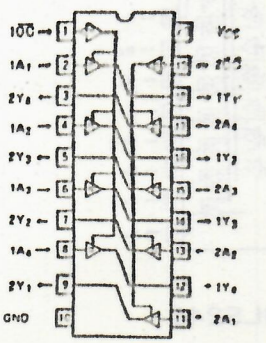
nted ring diagram of MAIN BOARD covers basic or representative here may be some component or partical circuit difference between and circuit diagram. The location numbers of this printed circuit he last three figures of the schematic location.
IC101)



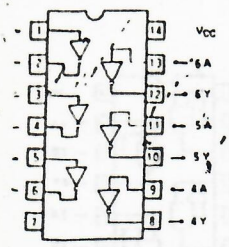

74LS00


74LS14


74LS139

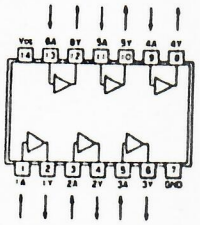

74LS244

IC BLOCK DIAGRAM



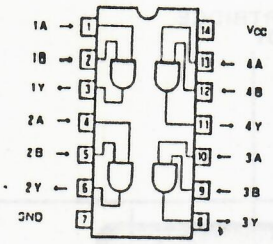
74LS04

7404 (open collector output)

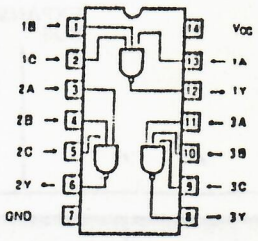


SN7407

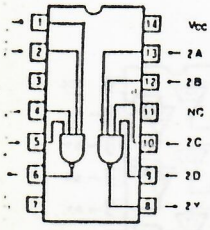
(open collector output)



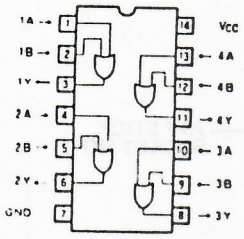
74LS08



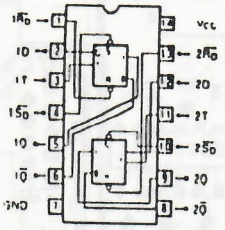
74LS10



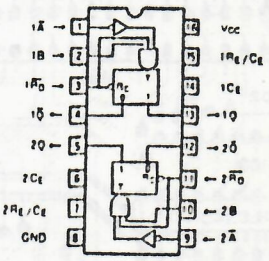
74LS20



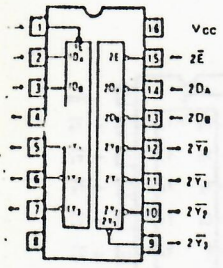
74LS32



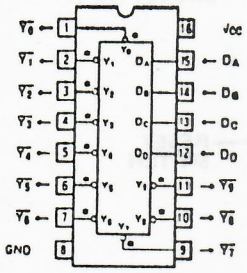
74LS74



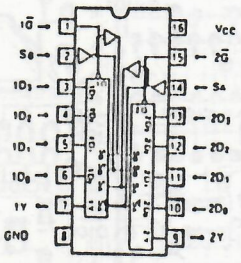
74LS123



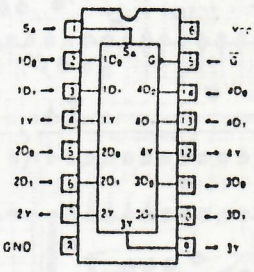
74LS139



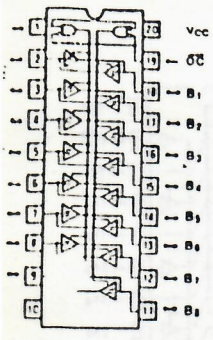
74LS145



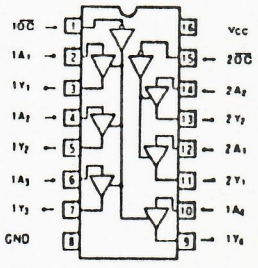
74LS153



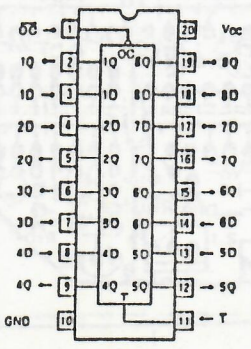
74LS157



74LS245

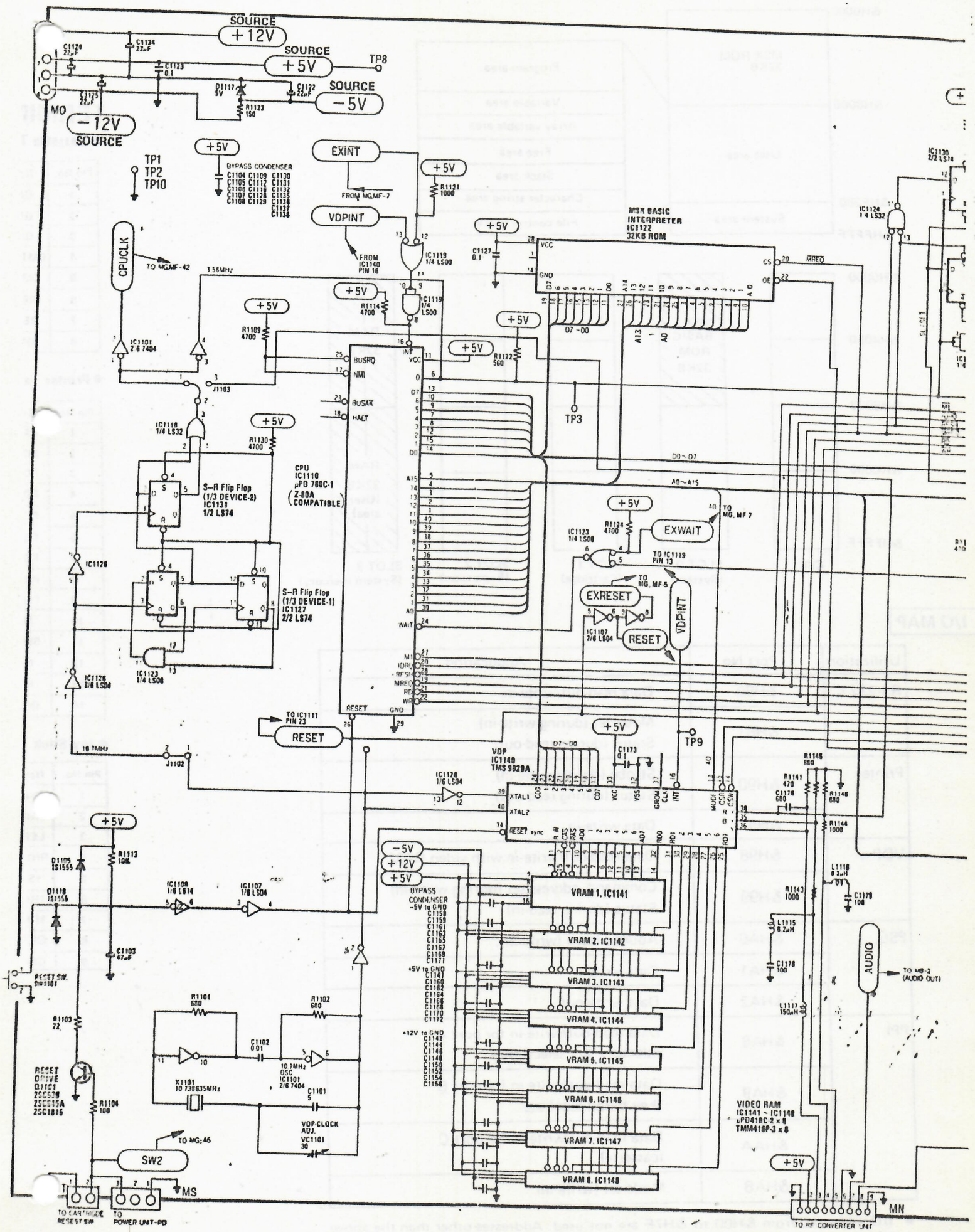


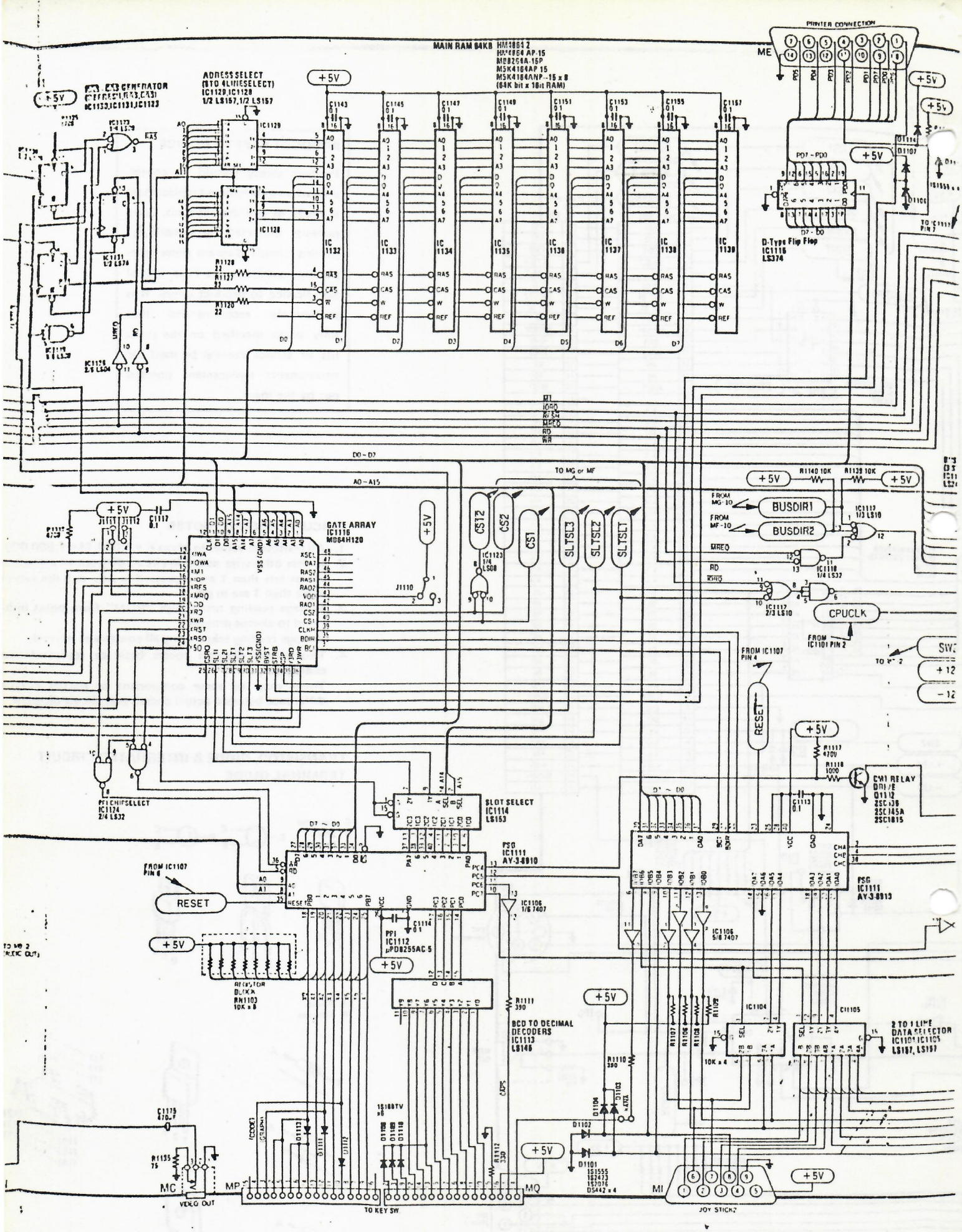
74LS367

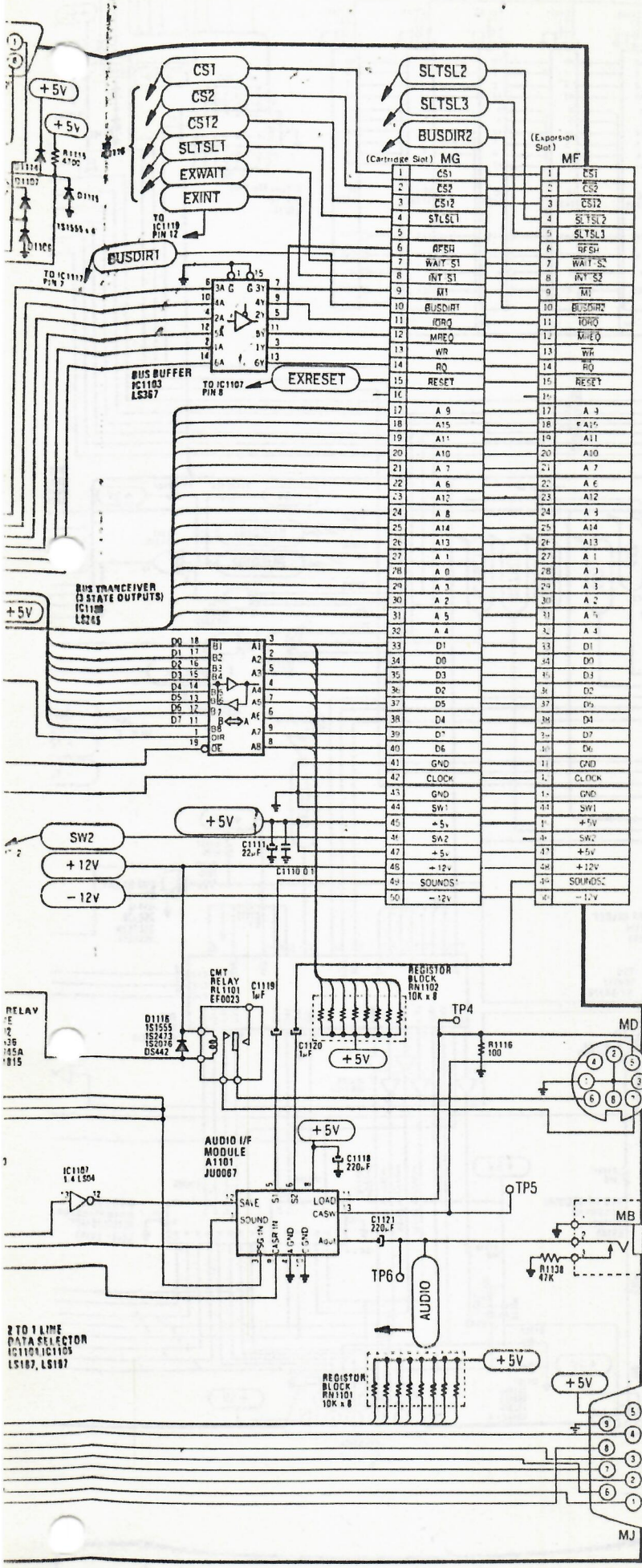


74LS374

CIRCUIT DIAGRAM OF MAIN BOARD




MAIN RAM 64KB
PRINTER CONNECTION
ADDRESS SELECT (BTO 4LINESELECT)
IC1129,IC1128
1/2 LS157,1/2 LS157
D-Type Flip Flop
IC1116
LS374
GATE ARRAY
IC1115
MB64H120
SLOT SELECT
IC1114
LS153
PSG
IC1111
AY-3-8910
PPI
IC1112
μPD8255AC-5
BCD TO DECIMAL DECODERS
IC1113
LS145
2 TO 1 LINE DATA SELECTOR
IC1101,IC1105
LS157, LS157
CPUCLK
RESET
BUSDIR1
BUSDIR2
JOY STICK2
TO KEY SW
VIDEO OUT



PRODUCT SAFETY NOTICE

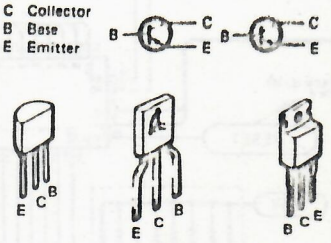
Product safety should be considered when a component replacement is made in any area of a set. Components indicated by a mark ⚠ in this circuit diagram show components whose value have special significance to product safety. It is particularly recommended that only parts specified on the parts list of service manual be used for components replacement pointed out by the mark.

CIRCUIT DIAGRAM NOTES:

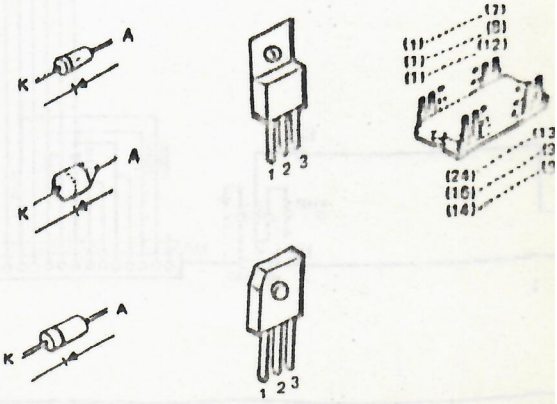
1. All resistance values in ohms K = 1,000, M = 1,000,000
2. Unless otherwise noted in circuit diagram all capacito values less than 1 are expressed in μF, and the value more than 1 are in pF.
3. Voltage reading taken with "VOM" from point indi cated to chassis ground.
   Voltage reading taken using all controls at normal.
4. This circuit diagram covers basic or representativ chassis only.
   There may be some component or partial circui difference between actual chassis and circuit diagram.

TRANSISTOR, DIODE & INTEGRATED CIRCUIT TERMINAL GUIDE

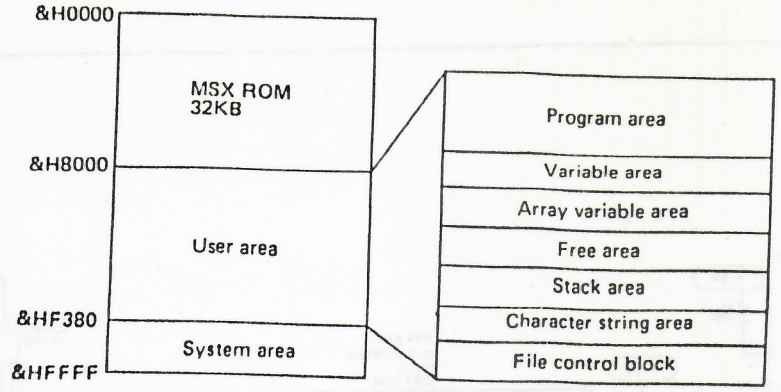
C Collector
B Base
E Emitter

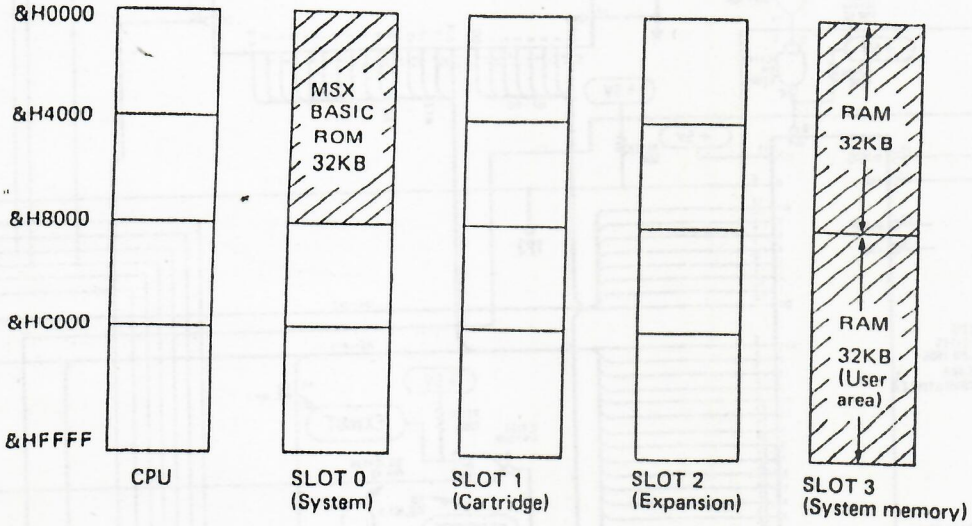


A Anode
K Cathode



MEMORY MAP





I/O MAP

Utilization	Port No.	Application
RS-232-C	&H80	Data read-out/write-in
	&H81	Mode set (during write-in) Status (during read-out)
Printer	&H90	Strobe (during write-in) Status (during read-out)
	&H91	Data write-in
VDP	&H98	Data read-out/write-in with video RAM.
	&H99	Command, address set (during write-in) Status (during read-in)
PSG	&HA0	Address latch (write-in)
	&HA1	Data write-in
	&HA2	Data write-out
PPI	&HA8	Data read-out/write-in for port A (Memory slot select) use.
	&HA9	Data read-out/write-in for port B (key borad scan) use.
	&HAA	Data read-out/write-in for port C (cassette).
	&HAB	Mode set (write-in)

- I/O addresses from &H00 to &H7F are not used Addresses other than the above addresses of the address among &H80 to &HFF are reserved for system use.

TERMI

- Cassette T

Pin No.	Na
1	GI
2	GI
3	GI
4	CMT
5	CM
6	RE
7	RE
8	GI

- Printer Te

Pin No.	Na
1	$\overline{ST}$
2	PD
3	PD
4	PD
5	PD
6	PD
7	PD
8	PD
9	PD
10	N
11	BU
12	N
13	N
14	GI

- Joy Stick

Pin No.	Nar
1	
2	
3	LEI
4	RIG
5	+5
6	TRI
7	TRI
8	OU
9	GN

TERMINALS SPECIFICATIONS

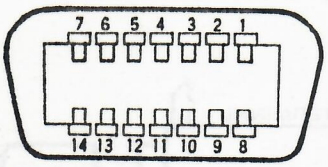
○ Cassette Tape Recorder Terminal

Pin No.	Name		Pin Connection
1	GND	–	
2	GND	–	
3	GND	–	
4	CMTOUT	Output	
5	CMTIN	Input	
6	REM+	Output	
7	REM–	Output	
8	GND	–	

(Seen from OUT side)

○ Printer Terminal

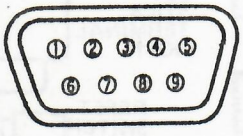
Pin No.	Name	Pin Connection
1	$\overline{\text{PSTB}}$	
2	PDB0	
3	PDB1	
4	PDB2	
5	PDB3	
6	PDB4	
7	PDB5	
8	PDB6	
9	PDB7	
10	NC	
11	BUSY	
12	NC	
13	NC	
14	GND	



(Seen from OUT side)

○ Joy Stick Terminal

Pin No.	Name		Pin Connection
1	FWD	Input	
2	BACK	Input	
3	LEFT	Input	
4	RIGHT	Input	
5	+5V	–	
6	TRG1	Output	
7	TRG2	Output	
8	OUT	Output	
9	GND	–	

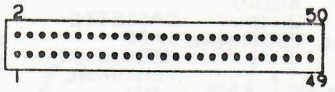


(Seen from OUT side)

• ROM Cartridge Slot/Expansion Bus

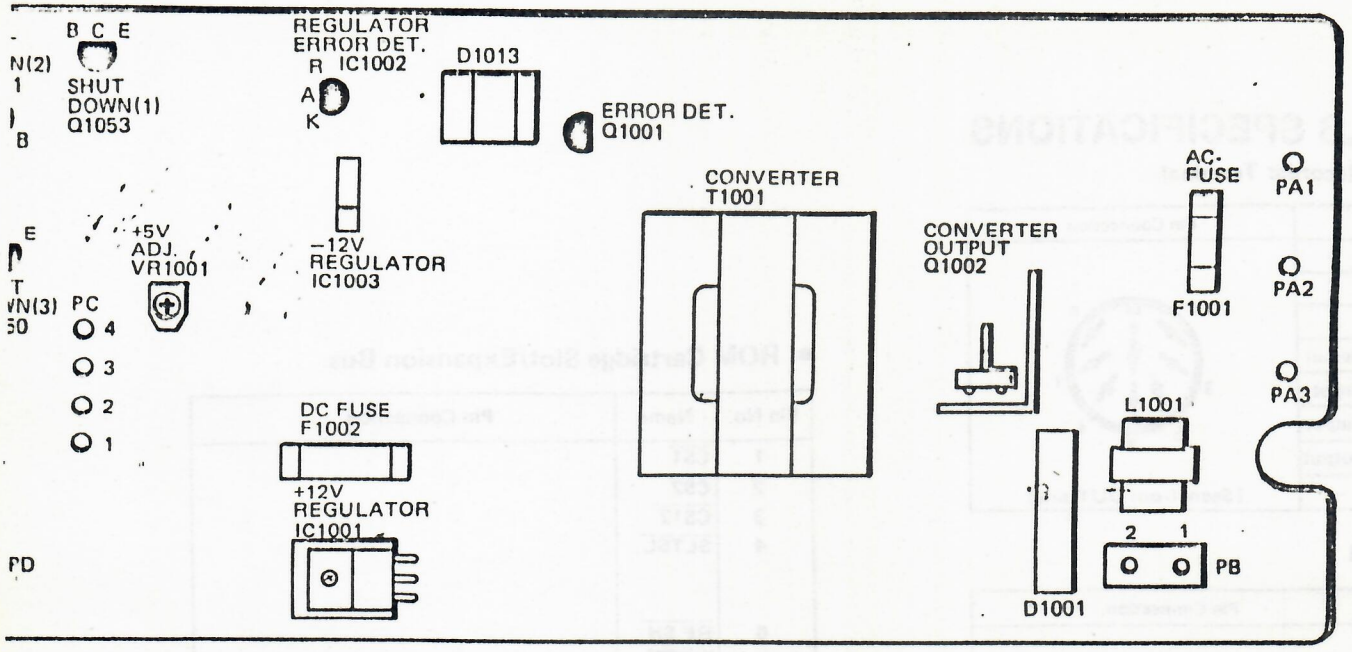
Pin No.	Name	Pin Connection
1	$\overline{\text{CS1}}$	
2	$\overline{\text{CS2}}$	
3	$\overline{\text{CS12}}$	
4	$\overline{\text{SLTSL}}$	
6	$\overline{\text{RF SH}}$	
7	$\overline{\text{WAIT}}$	
8	$\overline{\text{INT}}$	
9	$\overline{\text{MI}}$	
10	$\overline{\text{BUSDIR}}$	
11	$\overline{\text{IORQ}}$	
12	$\overline{\text{MERQ}}$	
13	$\overline{\text{WR}}$	
14	$\overline{\text{RD}}$	
15	$\overline{\text{RESET}}$	
17~32	A0~A15	
33~40	D0~D7	
41	GND	
42	CLOCK	
43	GND	
44, 46	SW1, SW2	
45, 47	+5V	
48	+12V	
49	SUNDIN	
50	–12V	

(Expansion Bus)



(Seen from OUT side)

ER BOARD



BOARD