Technical description of Carnivore2+

This is the detailed technical description and documentation for the multi-functional Carnivore2+ cartridge that was created by RBSC.

NOTE: The hexadecimal numbers are shown as `#90`, `90h` or `0x90`

The main components and features:

- External storage: CF card (CompactFlash), MicroSD card
  - Nextor is used as DOS (built–in support for FAT12/16, maximum partition size: 4 GB)
  - High read and write speeds
  - Supports SD and MicroSD card adapters
  - Nextor supports floppy disk emulation with DSK files
  - Utilities compatible with MSX-DOS versions 1 and 2
  - The cartridge can be configured as a RAM extension, disk drive, music or SCC/SCC+ sound card, FlashROM cartridge or a combination of these devices
- RAM: 2048 KB (2 MB)
  - Includes:
    - 1024 KB main RAM with mapper (default configuration)
    - 1024 KB Shadow RAM with a mapper, similar to MegaRAM (default configuration)
    - 2048 KB of RAM may be allocated to either main RAM with mapper or to Shadow RAM
    - 8 KB for the FMPAC SRAM (a backup battery is needed to save data after turning off the power)
    - 256 KB for the MSX Audio SRAM (for storing digital audio samples)
- Flash memory (FlashROM): 8 MB capacity, 64 Mbit/s
  - The first 394 KB are used for service information and ROM BIOSes
  - Mapper emulation:
    - Linear 64 KB mode
    - ASCII8
    - ASCII16
    - Konami4
    - Konami5 (SCC/SCC+)
    - Custom mapper
- Sound/music
  - PPI, PSG or Dual-PSG (I/O ports: 10h–11h or A0h–A1h)
  - Konami SCC and SCC+ emulation
  - OPLL emulation (YM2413, MSX – Music), BIOS IU translated to English
  - OPM emulation (YM2151, SFG-05, code by Jotego), original ROM BIOS
  - OPL emulation (Y8950, MSX Audio code by Jotego), original ROM BIOS
  - ADPCM sample playback support (for MSX Audio, code by RBSC)
  - SN7 (SN76489AN, code by Jotego) chip emulation
  - Volume setting for all emulated audio devices
  - SN7, PSG and PPI can be enabled and disabled in the user interface
- Additional features
  - EFU (Easy Firmware Updating) feature allows to upload firmware and music module's BIOS from any MSX computer
  - Boot menu with a choice of games and configurations saved in flash memory
    - Sorting of directory records
    - Customizable user interface (colors, sorting, key repeat speed, fade effects)
    - Help system
    - Joystick and joypads support
    - 50/60Hz instant switching support
    - Selectable Turbo or R800 modes
    - Auto-Start of configuration entries and ROMs with a startup delay
    - Allows to run 2 ROMs at the same time in the Dual-Slot screen
    - Mono/stereo modes for music module's output
    - Allows to set the default startup frequency (50 or 60Hz)
  - The device is designed in the form factor of the standard MSX cartridge
  - It operates at the standard frequency of 3.58 MHz, as well as turbo frequencies up to 7.11 MHz
  - Implemented on FPGA (EP2C8Q208C8N Altera Cyclone II)
  - Special software is used to control all functions
    - Download programs in ROM format to flash memory and RAM
    - Backing up flash memory, configuration RAM settings, and #C2SRAM|FMPAC RAM contents
    - Program for testing IDE, SD and floppy disk interfaces, etc
  - Easy setup and user–friendly interface

On–board BIOSes and modules:

File	Subslot	Description
BOOTCMFC.BIN	0	Boot Menu
BIDECMFC.BIN or SDSCCMFC.BIN	1	IDE ROM or SD ROM
RAM or SDSCCMFC.BIN or BIDECMFC.BIN	2	1 MB RAM or IDE/SD ROM
FMPCCMFC.BIN, SFGMCMFC.BIN, MSXACMFC.BIN or SDSCCMFC.BIN or BIDECMFC.BIN	3	MUSIC ROM or IDE/SD ROM

The location of the Boot Menu, directory and BIOSes in the FlashROM chip is described below. There are logical and physical blocks and they have different numbering.

The location of blocks in FlashROM

The FlashROM chip that is used in Carnivore2+ has 8 logical blocks in the first physical 64 KB block and then go the rest of 64 KB physical blocks. In the logical blocks there are Boot Menu and directory. The next few blocks are allocated for the BIOSes of the embedded devices.

8 KB blocks

The first 8 logical 8 KB blocks are grouped into the first physical block that is addressed by the AddrFr register. Logical blocks 0, 1, 4, 5, 6 and 7 contain the Boot Menu's code and data. Blocks 2 and 3 contain directory entries.

Address range	Block number	Description
000000h–001FFFh	0	contains Boot Menu's code; after power on (AddrFR=#00, R1Mult="10000101" B1AdrD = #4000) is visible in subslot 0 at address #4000–#5FFF and contains the first 8 KB of boot menu (ROM "AB" header + start addresses)
002000h–003FFFh	1	contains Boot Menu's code; after power on is visible in subslot 0 at addresses #6000-#7FFF (bits 2–0 of R1Mult = "101" are the size of the shown block (16 KB)) and contain the second 8 KB of boot menu
004000h–005FFFh	2	directory entries
006000h–007FFFh	3	directory entries
008000h–009FFFh	4	contains Boot Menu's code
00A000h–00BFFFh	5	contains Boot Menu's code
00C000h–00DFFFh	6	used for the data of the Boot Menu
00E000h–00FFFFh	7	used for the data of the Boot Menu

64 KB blocks

After the first 8 logical 8 KB blocks that form the first physical block, there go the physical 64 KB blocks of the FlashROM.

Address range	Physical block number	Logical block number	Description
010000h–01FFFFh	8	1, AddrFR=#01	contain the IDE BIOS
020000h–02FFFFh	9	2, AddrFR=#02	
030000h–03FFFFh	10	3, AddrFR=#03	contains FMPAC BIOS
040000h–04FFFFh	11	4, AddrFR=#04	contain the SD BIOS
050000h–05FFFFh	12	5, AddrFR=#05	

Address range	Physical block number	Logical block number	Description
060000h–7FFFFFh	134	127, AddrFR=#6-#7F	Data blocks — these blocks are used for saving the ROM images (games, etc.)

FlashROM chip

Model: Numonix M29W640GB TSOP48
Datasheet

Block layout:

#00000	8K
#02000	8K
#04000	8K
#06000	8K
#08000	8K
#0A000	8K
#0C000	8K
#0E000	8K
#10000	64K x 127

Command addresses: #4555 and #5AAA

Commands:

AUTOSELECT	#90
WRITE	#A0
CHIP_ERASE	#10
BLOCK_ERASE	#30
RESET	#F0

FlashROM ID: #7E

- Block 0 is reserved for the directory and the boot menu: `BOOTCMFC.BIN`
- Blocks 1–2 are reserved for the IDE BIOS: `BIDECMFC.BIN`
- Block 3 is reserved for MUSIC BIOS (`FMPCCMFC.BIN`, `SFGMCMFC.BIN`, `MSXACMFC.BIN`)
- Blocks 4-5 is reserved for SD BIOS (`SDSCCMFC.BIN`)

FMPAC (OPLL) and SRAM emulation

The OPLL emulation (FMPAC) that is supported by the cartridge is mapped to ports #7C–7D.

The FMPAC SRAM is emulated by reserving 8 KB in the upper part of the first half of Carnivore2+'s RAM. That area is not a part of normal RAM that is allocated for the system's use by default and it is located in the Shadow RAM. The physical location of this area in cartridge's RAM is #0FE000h–#0FFFFFh. The register #3A allows to disable SRAM's emulation or to move it to the second half or RAM: #1FE000h–#1FFFFFh.

NOTE: The settings of SRAM will be lost after powering down unless the cartridge has the backup battery installed.

FMPAC's own control registers:

- 7FF4h: write YM-2413 register port (write only)
- 7FF5h: write YM-2413 data port (write only)

- 7FF6h: activate OPLL I/O ports (read/write)
- 7FF7h: ROM page (read/write)

To enable 8 KB of SRAM at address 4000h–5FFFh, write #4D to address #5FFE and #69 to address #5FFF.

MSX Audio and SRAM emulation

The MSX Audio emulation is supported on ports #C0–#C1.

The MSX Audio's SRAM is emulated by reserving 256kb in the upper part of the first half of Carnivore2+'s RAM. That area is not a part of normal RAM that is allocated for the system's use by default and it is located in the Shadow RAM. The physical location of this area in cartridge's RAM is #0C0000h–#0FFFFFh. The register #3A allows to disable SRAM's emulation, or to move it to the second half or RAM: #1C0000h–#1FFFFFh.

Also, alternative ports for MSX Audio emulation are supported: #C4-#C5, the register #3A allows to switch to alternative ports.

Additional configuration EEPROM

Model: M93C46MN1 (128 bytes/1 Kbit)
Datasheet

IMPORTANT! The chip is operated only in 8–bit mode!

This EEPROM is used to store additional configuration settings. Using the EEPROM prevents the important configuration settings from being lost after power goes down. The location of the settings in the EEPROM and their description can be found i the table blow.

Address	Description
01	FMPAC and SCC volume, 3 bits per value, max volume is 8, first 2 bits are used as flags
02	50 or 60 Hz VDP frequency flag, bit 1 from this byte is used — if this bit is zero then 60 Hz is used
03	PSG and clicker enable/disable flags and volumes, 3 bits per volume, max volume is 8, first 2 bits are used as enable/disable flags
04	Entry sorting (0=disabled)
05	Fade in/out effects (0=disabled)
06	Keyboard/joystick speed (this is an increment for default value)
07	Menu font palette
08	
09	Menu background palette
0A	
0B	Help font palette
0C	
0D	Help background palette
0E	
0F	Volume font palette
10	
11	Volume background palette
12	
13	PSG/PPI font palette
14	

Address	Description
15	PSG/PPI background palette
16	
17	Custom settings in use flag (must be #42)
18	Double reset on “cold boot” (1=enabled)
19	FMPAC mono (1=enabled)
1A	Last used entry
1B	Music playback status
1C	Autostart entry number
1D	Help scroller status
1E	Dual-PSG status
1F	Autostart delay
20	Slot 3 usage flag
21	User-configurable ID and control port number

Writing to EEPROM is done via the configuration register `CardMDR+#23`. The commands for EEPROM are saved into this register in a sequence that is described in the chip's datasheet. Only write–enable, read and write commands are used.

Configuration registers

The configuration registers are located at addresses #0F80 or #4F80 or #8F80 or #CF80h. Their visibility and location is controlled by the main control register's first byte — at address #4F80. The main control register is called `CardMDR`. After power on, the registers are located at address #4F80. All registers are write–only except the pseudo–register for sending/receiving the data when accessing the FlashROM and the register for the configuration EEPROM, as well as 3 bytes of the firmware version - FPGA_ver.

Below you can find the description of configuration registers.

Register number, name	Bit number	Value	Description
00 CardMDR	Main cartridge's configuration register		
01 AddrM0	lower address register (bits 7–0) for accessing the FlashROM		
02 AddrM1	middle address register (bits 15–8) for accessing the FlashROM		
03 AddrM2	higher address register (bits 22–16) for accessing the FlashROM		
04 DatM0	pseudo–register for sending/receiving data from/to FlashROM		
05 AddrFR	register controlling the number of FlashROM's 64 KB block for ROM emulation The default value of this register is 00h		
06 R1Mask	Configuration registers for bank 1		
07 R1Addr			
08 R1Reg			
09 R1Mult			
0A B1MaskR			
0C R2Mask	Configuration registers for bank 2		
0D R2Addr			
0E R2Reg			
0F R2Mult			
10 B2MaskR			
11 B2AdrD			

Register number, name	Bit number	Value	Description
12 R3Mask	Configuration registers for bank 3		
13 R3Addr			
14 R3Reg			
15 R3Mult			
16 B3MaskR			
17 B3AdrD			
18 R4Mask	Configuration registers for bank 4		
19 R4Addr			
1A R4Reg			
1B R4Mult			
1C B4MaskR	similar to B1MaskR		
1D B4AdrD	similar to B1AdrD		
1E Mconf	Expanded slot configuration register		
1F CMDRCpy	copy of the CardMDR+#00 register (to be used with LDIR command)		
20 ConfFl	FlashROM chip's configuration The default value of this register is — 010b		
	2	0	8 bit bus
		1	16 bit bus
	1	Reset/protect flag	
	0	1	enable 12V for boosted writing into FlashROM
		0	ɜdisable 12V for boosted writing into FlashROM
21 NSReg	Non-standard Register The default value of this register is #00, please don't change it!		
22 SndLVL	volume level register The default value of this register is 1Bh (00011011b)		
	7, 6	10 = FMPAC mono, 00 = FMPAC stereo	
	5, 4, 3	FMPAC audio level (0–7)	
	2, 1, 0	SCC/SCC+ audio level (0–7)	
23 CfgEEPR	register for controlling additional configuration EEPROM (93C46)		
	7, 6, 5, 4	not used	
	3	EECS signal Chip Select EEPROM	
	2	EECK signal CLK (sync)	
	1	EEDI signal Data Input (data sent to EEPROM)	
	0	EEDO signal Data Output (data received from EEPROM); read–only	
24 PSGCtrl	PSG control register The default value of this register is 1Bh (00011011b)		
	7	enable/disable PSG	
	6	enable/disable PPI Clicker	
	5, 4, 3	PSG audio level (0–7)	
	2, 1, 0	PPI Clicker audio level (0–7)	
25	DEACTIVATED! low byte of interceptor's address		
26	DEACTIVATED! high byte of interceptor's address		
27	DEACTIVATED! interceptor's configuration for delayed start		

Register number, name	Bit number	Value	Description
	0	activation flag for interceptor code on system restart or read from #4000	
		1	enabled
	1	interceptor code's location	
		0	boot menu in FlashROM
		1	first shadow RAM block
28 SLM_cfg	per–device subslot assignment (master slot)		
	7	FMPAC subslot number	
	6		
	5	RAM (Mapper MMM) subslot number	
	4		
	3	IDE (CF) subslot number	
	2		
	1	FlashROM/SCC subslot number	
	0		
29 SCART_cfg	slave slot control register		
	7	1	slave slot enabled
		0	slave slot disabled
	6	1	slave slot's location assigned by user
		0	slave slot assigned as subslot of master slot
	5	1	slave slot expanded (if not used as a subslot of master slot)
		0	slave slot non–expanded (if not used as a subslot of master slot)
	4	1	master slot's location is assigned by user
		0	master slot located at the physical slot
	3	1	not used
		0	
	2	1	allow slot select register for emulated slot (used only for slots 1 and 2)
		0	disable slot select register for emulated slot (real slot's register will be used)
2A SCART_SLT	slot/subslot configuration on power–on		
	7, 6	00 = mini ROM up to 32 KB without mapper 01 = K4 mapper 10 = K5 mapper without SCC 11 = K5 mapper + SCC	
	5, 4	master slot number	
	3, 2	expanded slave slot number	
	1, 0	slave slot number	
2B SCART_StBl	slave slot's 64 KB block assignment in FlashROM		
2C, 2D, 2E FPGA_ver	FPGA firmware version (3 ASCII bytes)		
2F	MROM_offs = mini ROM offset in 64 KB block (in 8 KB steps)		
30 PSGAlt	PSG port configuration		
	1	reserved	
	0	1	alternative ports: #10-#11
		0	default ports: #A0-#A1
35 PFXN	User-configurable I/O port number for ID and control		

Register number, name	Bit number	Value	Description
36 SD_SLT_CFG	SD Device Slot Configuration		
	7	SD interface is active	
	6	0	Sunrise IDE interface is active
		1	substitute slot number for use with IDE, bits 1,0 - number of slot to substitute the initial configuration (upon restart) SD_SLT_CFG depends on whether SD is inserted; #81 if SD is inserted, #01 if SD is not inserted
37 SFL_CFG	SFL Control (Serial flash for CPLD loading)		
	7	1	enables serial EEPROM's mapping
	5	1	allows JTAG to control EEPROM's pins (zeroed if we want to control ourselves)
	3	controls nCS chipselect, low-active	
	2	1	manual pin control is disabled
		0	EEPROM control by software
38 CMUZM	Config/variant Music Module (expanded slot 3)		
	0	MUSIC module's selection (read-only): 000 - FMPAC, 001 - SFG, 010 - MSX Audio	
	1		
	2		
	3	0 - SFG-01 BIOS; 1 - SFG-05 BIOS (low or high 32kb of BIOS are selected)	
	5	SN76489AN emulation control (JT-89 implementation). 00 - SN76489AN is controlled via 803Ch / 403Ch MMM (Musical Memmory Mapper) register of the catridge by default 01 - emulation is off. 10 - always enabled and is controlled via MSX port #03F. 11 - reserved	
	4		
39 LVL2	volume level for SN76489AN emulation		
3A RAMuv	RAM layout and SRAM options (by default 000)		
	0	= 0 - 1 MB for RAM, 1 MB for Shadow RAM = 1 - 2 MB for RAM or Shadow RAM; if RAM is disabled in register #1F, then all 2 MB are assigned for Shadow RAM	
	1	= 0 - FMPAC SRAM is located in the first half of RAM (address range 0FE000-0FFFFF), ExtRAM (sample RAM) is located at 0C0000h-0FFFFFh	
		= 1 - FMPAC SRAM is located in the second half of RAM (address range 1FE000-1FFFFF), ExtRAM (sample RAM) is located at 1C0000h-1FFFFFh	
	2	= 0 FMPAC SRAM or ExtRAM (sample RAM) is enabled	
		= 1 FMPAC SRAM or ExtRAM (sample RAM) is disabled	
	3	= 0 standard Y8950 (MSX-Audio) ports: #C0, #C1	
		= 1 alternative Y8950 ports: #C4, #C5	
	4	= 0 Y8950 OPL + ADPCM output	
		= 1 only Y8950 OPL output (ADPCM is off)	

Registers of configuration bank

There are six bank configuration registers:

1. RnMask
2. RnAddr
3. RnReg
4. RnMult

5. BnMaskR
6. BnAdrD

n — this is the bank number.

RnMask

Bitmask for bank's register address. This value is normally mirrored into several addresses, for example for Konami 5 cartridges those addresses for the first bank are 5000h–57FFh. Here we use only the high byte's address — F8h (11111000b).

The default value of this register is F8h

RnAddr

High byte of the bank's address register (example: 50h for address 5000h)

The default value of this register is 50h.

RnReg

Initial value for bank's number (usually 00h)

The default value of this register is 00h.

RnMult

RnMult — bank's mode and size register

Bit number	Value	Description
7	1	bank's register is enabled
	0	bank's control is disabled
6	1	mirroring is disabled
	0	mirroring is enabled
5	media type selection	
	0	FlashROM
	1	RAM
4	1	writing to bank is enabled
	0	writing to bank is disabled
3	0	bank is enabled
	1	bank is disabled
2, 1, 0	bank's size 111b = 64 KB, 110b = 32 KB, 101b = 16 KB, 100b = 8 KB, 011b = 4 KB other value — bank is disabled The default value of this register is 85h	

The default value is 00h (bank is disabled)

BnMaskR

Bitmask for bank's addressing mode into the FlashROM. This is the ROM's emulated size and the number of pages. For example for a 128 KB ROM we will need 16 pages of 8 KB, so we set the 0Fh (00001111b) mask.

The default value of this register is 03h

BnAdrD

High byte of the bank's address (example: 40h for address 4000h).

The default value of this register is 40h

CardMDR

00 CardMDR — main cartridge's configuration register

Bit number	Value	Description
7	1	don't show registers
	0	show registers
6	0/1/2/3	registers are located at addresses 0F80h/4F80h/8F80h/CF80h
5		
4	1	SCC enabled
	0	SCC disabled
3	1	delayed configuration
	0	configuration is changed immediately after updating the registers
2	0	delayed configuration is enabled after CPU executes at address 0000h
	1	configuration is enabled after reading from address 4000h The delayed configuration works only for AddrFR and bank control registers
1	source for BIOS of embedded devices	
	0	BIOS data (Boot Menu, DISK module, MUSIC module) is read from FlashROM chip
	1	BIOS data (Boot Menu, DISK module, MUSIC module) is read from RAM Warning! The data must be copied into DAM before setting this bit!
0	configuration registers visibility control	
	0	all configuration registers are visible at addresses 0F80h/4F80h/8F80h/CF80h depending on the values of bits 5 and 6
	1	configuration registers are not visible, 1 byte of data from the corresponding block in the FlashROM is available at those addresses

Mconf

1E Mconf — expanded slot configuration register

Bit number	Value	Description
7	1	slot is expanded (bits 0-3 set what devices are active)
	0	slot is not expanded (the first device with active bit will be used)
6	1	enable reading of MMM mapper's ports #FC, #FD, #FE and #FF
	0	port reading is disabled

Bit number	Value	Description
5	1	enable MUSIC module (FMPAC, SFG or MSX Audio)
	0	MUSIC module is disabled
4	1	enable MMM memory mapper's control on port #3C
	0	MMM mapper is disabled
3	1	enable MUSIC module in subslot x.3
	0	subslot is not used
2	1	enable MMM mapper in subslot x.2
	0	subslot is not used
1	1	enable DISK module in subslot x.1
	0	subslot is not used
0	1	enable SCC and FlashROM in subslot x.0
	0	subslot is not used

Directory entry format

There are 253 user–controlled directory entries available in the cartridge. The first directory entry can't be edited or deleted because it sets the default cartridge's configuration — all enabled. The directory is 8 KB in size and is located in the 2 and 3 logical blocks of the FlashROM chip at addresses 004000h–005FFFh (block 2) and 006000h–007FFFh (block 3). The physical block number (controlled by the `AddrFr` register) is zero.

Each directory entry occupies 40h (64 bytes) and has the following format:

Register number	Name	Bit number	Value/description
#00	NUM	Record number (last one — #FF is ignored)	
#01	ACT	Active/empty record's flag (#FF — active record)	
#02	STB	Starting 64 KB block for data	
#03	LNB	Data size in 64 KB blocks	
#04	MAP	Mapper type symbol	
#05	NAM	Record name (30 bytes)	
#22	NAM		
#23	R1Mask	Configuration registers for bank 1	
#24	R1Addr		
#25	R1Reg		
#26	R1Mult		
#27	B1MaskR		
#28	B1AdrD		
#29	R2Mask	Configuration registers for bank 2	
#2A	R2Addr		
#2B	R2Reg		
#2C	R2Mult		
#2D	B2MaskR		
#2E	B2AdrD		

Register number	Name	Bit number	Value/description
#2F	R3Mask	Configuration registers for bank 3	
#30	R3Addr		
#31	R3Reg		
#32	R3Mult		
#33	B3MaskR		
#34	B3AdrD		
#35	R4Mask	Configuration registers for bank 4	
#36	R4Addr		
#37	R4Reg		
#38	R4Mult		
#39	B4MaskR		
#3A	B4AdrD		
#3B	Mconf	expanded slot configuration register	
#3C	CardMDR	main configuration register	
#3D	PosSiz	size and position in 64 KB block for mini ROMs	
#3E	RstRun	reset and start options	
#3F	Resrv	Reserved	

PosSiz

PosSiz — size and position in 64 KB block for mini ROMs

Bit number	Value/description
7	reserved
6, 5, 4	offset of mini ROM in 64 KB block based on ROM's size:
3	non–standard ROM size: 1 — 49 KB 0 — standard ROM size
2, 1, 0	mini ROM's size: 110b = 32 KB 101b = 16 KB 100b = 8 KB 011b = 4 KB 000b = not mini ROM

	8 KB	16 KB	32 KB
000b	0 KB	0 KB	0 KB
001b	8 KB	16 KB	32 KB
010b	16 KB	32 KB	
011b	24 KB	48 KB	
100b	32 KB		
101b	40 KB		
110b	48 KB		
111b	56 KB		

RstRun

RstRun — reset and start options

Bit number	Value/description
3	ROM's start address: 0 — use bit 2 from this register 1 — use start address at 0002h
2	ROM's start address: 0 — use start address at 4002h 1 — use start address at 8002h
1	execution control: 0 — don't start ROM 1 — start using ROMini address (bits 3,2)
0	reset flag: 0 — do not reset MSX 1 — reset MSX

Mappers

The cartridge supports a few common mappers and the linear mode that allows first 64 KB of the MiniROM to be visible in the address space. The physical addresses allocated for the mappers' operation lie in the range of 100000h–1FFFFFh. This means that only the second megabyte of RAM is used.

Mappers type values:

K	Konami5 (SCC) mapper
k	Konami4 mapper
a	ASCII8 mapper
A	ASCII16 mapper
M	mini ROM (8, 16, 32, 48 and 64 KB ROM without mapper)
C	configuration entry
U	unknown mapper

ASCII8

The cartridge supports the ASCII8 mapper.

Default configuration values:

#F8	#60	#00	#84	#FF	#40	**bank 1**
#F8	#68	#00	#84	#FF	#60	**bank 2**
#F8	#70	#00	#84	#FF	#80	**bank 3**
#F8	#78	#00	#84	#FF	#A0	**bank 4**
#FF	#AC	#00	#02	#FF		**configuration registers**

ASCII16

The cartridge supports the ASCII16 mapper.

Default configuration values:

#F8	#60	#00	#85	#FF	#40	**bank 1**
#F8	#70	#00	#85	#FF	#80	**bank 2**
#F8	#60	#00	#85	#FF	#C0	**bank 3**
#F8	#70	#00	#85	#FF	#00	**bank 4**
#FF	#8C	#00	#01	#FF		**configuration registers**

Konami4

The cartridge supports the Konami4 mapper.

Default configuration values:

#F8	#50	#00	#04	#FF	#40	**bank 1**
#F8	#60	#01	#84	#FF	#60	**bank 2**
#F8	#80	#02	#84	#FF	#80	**bank 3**
#F8	#A0	#03	#84	#FF	#A0	**bank 4**
#FF	#AC	#00	#02	#FF		**configuration registers**

Konami5

The cartridge supports the Konami5 (SCC) mapper.

Default configuration values:

#F8	#50	#00	#84	#FF	#40	**bank 1**
#F8	#70	#01	#84	#FF	#60	**bank 2**
#F8	#90	#02	#84	#FF	#80	**bank 3**
#F8	#B0	#03	#84	#FF	#A0	**bank 4**
#FF	#BC	#00	#02	#FF		**configuration registers**

MiniROM

The cartridge supports MiniROM (ROM images up to 49 KB) without mapper.

Default configuration values:

#F8	#60	#00	#06	#7F	#40	**bank 1**
#F8	#70	#01	#08	#7F	#80	**bank 2**
#F8	#70	#02	#08	#3F	#C0	**bank 3**
#F8	#78	#03	#08	#3F	#A0	**bank 4**
#FF	#8C	#07	#01	#FF		**configuration registers**

Linear 64 KB mode

The cartridge supports the linear 64 KB mode, when the first 64 KB of the ROM are visible in the address space.

The default configuration values for MiniROMs are:

#F8	#60	#00	#06	#7F	#40	**bank 1**
#F8	#70	#01	#08	#7F	#80	**bank 2**
#F8	#70	#02	#08	#3F	#C0	**bank 3**
#F8	#78	#03	#08	#3F	#A0	**bank 4**
#FF	#8C	#07	#01	#FF		**configuration registers**

Bank addresses in linear mode:

#0000–#3FFF	**bank 1**
#4000–#7FFF	**bank 2**
#8000–#BFFF	**bank 3**
#C000–#FFFF	**bank 4**

Default register values

Below you can find the default values for several configuration registers.

CardMDR	CardMDR+#00	20h (but may vary because of 2 last bits)
AddrFR	CardMDR+#05	00h
R1Mult	CardMDR+#09	85h
R2Mult	CardMDR+#0F	00h
R3Mult	CardMDR+#15	00h
R4Mult	CardMDR+#1B	00h
CMDRCpy	CardMDR+#1F	20h
ConfFl	CardMDR+#20	02h

RCP file format

RCP file format description.

Address (byte)	Description	
#00	Mapper type	
#01	R1Mask	Configuration registers for bank 1
#02	R1Addr	
#03	R1Reg	
#04	R1Mult	
#05	B1MaskR	
#06	B1AdrD	
#07	R2Mask	Configuration registers for bank 2
#08	R2Addr	
#09	R2Reg	
#0A	R2Mult	
#0B	B2MaskR	
#0C	B2AdrD	
#0D	R3Mask	Configuration registers for bank 3
#0E	R3Addr	
#0F	R3Reg	
#10	R3Mult	
#11	B3MaskR	
#12	B3AdrD	

Address (byte)	Description	
#13	R4Mask	Configuration registers for bank 4
#14	R4Addr	
#15	R4Reg	
#16	R4Mult	
#17	B4MaskR	
#18	B4AdrD	
#19	Mconf	
#1A	CardMDR	
#1B	PosSiz	
#1C	RstRun	
#1D	Not used, always FF	

User-defined ID and control port I/O

Carnivore2+ can be detected and controlled via its own configurable port #F0-F2. The following I/O operations are possible:

1. Detection of the cartridge
    - Write “C” to port, then read the value. Carnivore2 will respond with its version - “2” (ASCII format). Carnivore2+ will respond with its version - “3” (ASCII format)
2. Identify the slot used by Carnivore2+
    - Write “S” to port, then read the value. Carnivore2+ will respond with its slot, for example “1” (ASCII format)
3. Hide control registers
    - Write “H” to port, the control registers will be hidden
4. Show control registers
    - Write “R” to port, control the registers will appear at their defined location (see below)
5. Set location for control registers
    - Write “0” to port, the control registers will appear at #0F80
    - Write “1” to port, the control registers will appear at #4F80
    - Write “2” to port, the control registers will appear at #8F80
    - Write “3” to port, the control registers will appear at #CF80
6. Set cartridge's device configuration (software reset is required!)
    - Write “A” to port, the cartridge will enable only the main slot (one device only)
    - Write “M” to port, the cartridge will set the default configuration (all devices enabled)

Cartridge testing utility

The special utility was created to test Carnivore2 and Carnivore2+ cartridges, it's called `c2tester`. The utility allows to erase and test the main FlashROM, configuration EEPROM and to test the on-board RAM (entire 2 MB). The testing of EEPROM and FlashROM is performed with bit tests (4 different values are written) or with address tests (the lower byte of byte's the address is written).

The tested cartridge must be inserted into the SECOND slot! The first slot must have Carnivore2 or Carnivore2+ cartridge that runs tests.

Below you can find the testing instructions.

—————————— THE UTILITY IS NOT A PART OF REPOSITORY ——————————

IMPORTANT!

It is strongly advised to erase the FlashROM chip using the special erasing option in the utility before running any tests on the FlashROM!

Please remove CF or/and SD cards from the cartridge before testing!

IMPORTANT!

The C2TESTER utility tests Carnivore2 or Carnivore2+ cartridges on-board RAM (2MB), FlashROM (8MB) and configuration EEPROM (128 bytes). ALL TESTS ARE DESTRUCTIVE! So please make sure to backup the FlashROM and configuration EEPROM's contents onto CF or SD cards!

The tested cartridge MUST NOT BE USED by the system! This means that if a system uses the tested cartridge's RAM, this will result in a crash diring the RAM test.

The tested cartridge should be put in cartridge slot 2 and the system should be booted from Carnivore2/2+ cartridge in slot 1. This way the cartridge in slot 2 could be tested without a problem.

It's possible to also put a RAM expansion cartridge in slot 1 and the tested cartridge in slot 2. The C2TESTER program should be then run from a diskette in a floppy drive. Running the utility from the tested cartridge's CF or SD card is not recommended. It's even better to remove SD or CF card from the tested cartridge to avoid conflicts and to boot from another device.

When two Carnivore2/2+ cartridges are present in a system, please make sure to input the slot number for the tested cartridge in slot 2 by typing “20” when C2TESTER asks for the slot number. Even if slot autodetection only shows the cartridge in slot 1, always input the number for the second slot.

If the FlashROM chip on the tested cartridge is not detected at program's startup, it can't be tested. However, it's still possible to test the RAM and the configuration EEPROM of that cartridge.

Please input slot numbers very carefully because entering the wrong slot number may result in destruction of data on the primary cartridge instead of the one that was supposed to be tested.

The full FlashROM test takes around 20 minutes, the full RAM test takes around 5 minutes. The configuration EEPROM test takes just a few seconds. Long tests could be stopped by holding ESC key. After the full set of tests the cartridge will be in the vanilla state (the FlashROM and EEPROM will be filled with 0xFF).

All pattern tests are performed with 4 different binary values: 00000000, 10101010, 01010101 and 11111111. This ensures that all bits are tested. The address consistency tests are performed with the byte values that correspond to the addresses, for example, byte at address 0x00 will be 0x00, byte at address 0xFF will be 0xFF. There's also a reverse consistency test that inverts byte values, so that at address 0x00 the byte value will be 0xFF.

In case of any failure, the test program will show the physical address where the failure occured, as well as the expected and actual byte values.

———————————— THE UTILITY IS NOT A PART OF REPOSITORY ————————————

The utility is provided at the sole discretion of RBSC.

https://sysadminmosaic.ru/en/msx/carnivore2p/specification

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