PROGRAMMABLE MIXING OF COLOR GRAPHICS AND EXTERNAL VIDEO USING NEW LSI DISPLAY PROCESSOR

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ABSTRACT

The mixing of two video sources up to now has been accomplished by using discrete analog components. The new LSI video display processor (VDP) is the first integrated circuit with the provision for mixing, under software control, an external composite video signal with its own 15 color single pin composite video. The mechanics of this interface and its implications are discussed.

INTRODUCTION

Adding two video signals together can display a powerful amount of information on a single screen. Such applications may involve education, business, or entertainment areas. As the television becomes more of an information center, using it for display of various data is expanding. With the advent of teletext and the blossoming of color graphics for business use, it was only natural that LSI integrated circuits be used for low cost displays. One of the features is to mix two video signals together. The architecture of the VDP supports this hardware and software interface.

ARCHITECTURE

One of the primary considerations for such a system in a consumer area is the cost. The amount of logic must be reduced to the minimum. The tradeoffs of cost versus features must be weighed. So it was chosen to deal with the video at the composite video level rather than at the luminance, chrominance, or color difference level. This would allow the minimization of pin count and a reduction in the amount of multiplexers to implement the mixing function. Another requirement was to preserve the external image as much as possible, for example the flesh tones should be preserved.

This suggests that the external video source be responible for providing the color burst to the target television. This then implies that the video display processor must have its color generation synchronized to the external colors. The horizontal and vertical syncs of each video source must also be synchronized to one another. Thus the mechanism of synchronization must be included in the design.

In order to explain the software end of the interface, it is necessary to briefly explain the workings of the rest of the VDP. The color image is ultimately formed from the reading of a display memory that is written to via a microprocessor. Developed internal to the chip is a four bit bus that permits a possible sixteen colors. One of these codes has been allocated for the transparent color. This allows manipulation of images on the different VDP planes to create three dimensional effects. When ever the transparent color is programmed the next image plane will show through. The final image plane is that formed by the external video and when the VDP is so programmed the external video plane will show through. Thus complex interactive graphics may be performed under full program control.

It is interesting to note that the external video source may originate from

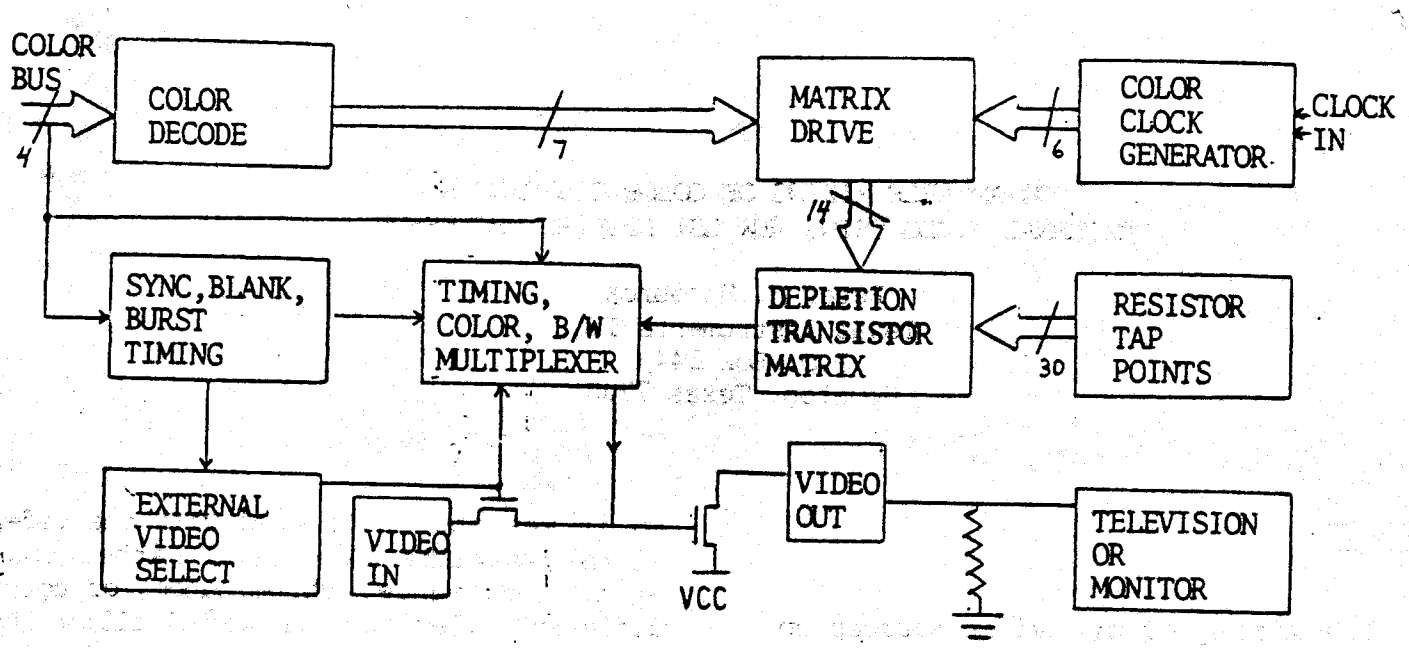


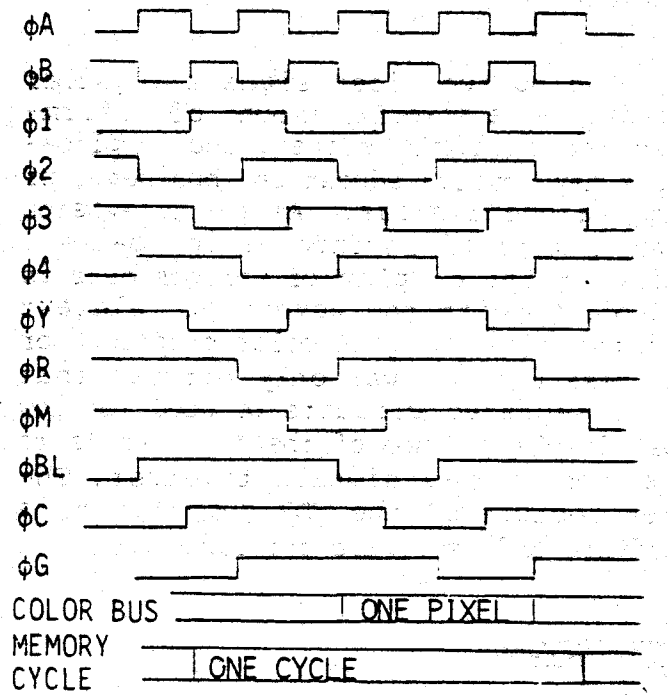
FIGURE 1 BLOCK DIAGRAM OF INTERNAL VIDEO CIRCUIT

another VDP. This chip is thus its own peripheral.

HARDWARE

Figure 1 illustrates the internal circuit of the VDP, both the generation of the composite video and the external video gating. The composite video is generated from a resistor tap selected by the decoded 4 bit color bus, the sync, blank, and color burst timing, and the six 3.58 Mhz color clocks which form the six chroma levels of yellow, red, magenta, blue, cyan, and green. The color bus is switching at a 5.3 Mhz rate and thus a horizontal resolution of 256 pixels per line is achieved. Figure 2 shows the timing of the color generation. The external video is a simple multiplexer gate that is logically opened by the proper conditions.

Figure 3 shows the system configuration to interface the VDP to a broadcast signal. The color subcarrier of the external video must be maintained in phase with the VDP's color subcarrier. To do this a phase locked loop is required to generate a 10.7 Mhz input clock (three times the subcarrier frequency) that the VDP divides down for its color generation. The loop is



φA - φB 10.73 MHZ CLOCK INPUTS (÷1)
φ1 - φ4 5.37 MHZ LOGIC CLOCKS (÷2)
φY - φG 3.58 MHZ COLOR CLOCKS (÷3)

FIGURE 2 TIMING DIAGRAM OF VDP CLOCKS

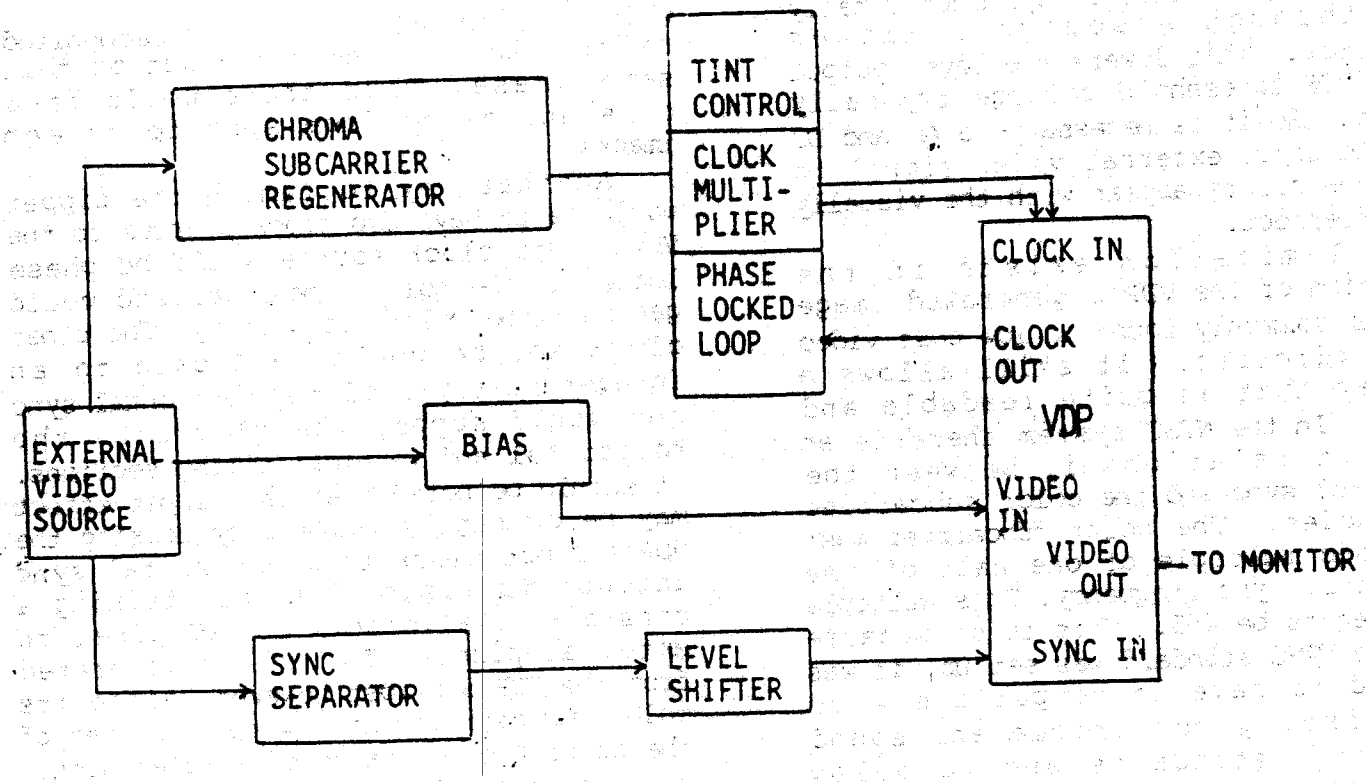


FIGURE 3 BLOCK DIAGRAM OF EXTERNAL VIDEO SYSTEM

completed with the 3.58 Mhz square wave output (phase equivalent to red), thus phase locking the two video subcarriers together. A tint control may be inserted as a delay in the 10.7 Mhz input clocks to vary the VDP's colors.

The horizontal and vertical sync is maintained through supplying composite sync to the VDP. This is done through a tri-level input pin that is shared with the VDP reset function. A 0 volt level represents reset, a 5 volt level is inactive, and a 12 volt level serves the sync function. By stripping off composite sync from the external video signal and level shifting it to provide a 5 volt to 12 volt positive going sync, the VDP maintains sync. The external sync is actually controlling the internal VDP timing.

The external sync signal is decoded by the VDP so that any positive going edge is sensed as a horizontal sync pulse. This resets the internal horizontal counter to a state that corresponds to its normal sync state time. This not only allows the VDP to be horizontally synchronized to the external video but also ensures that the VDP's external video gate will be opened up so that the external video's sync, blank, and burst will pass through and thus control the television.

A sync pulse that is longer than 7.2 microseconds is interpreted as a vertical sync. The VDP's internal vertical counter is reset to its normal sync state and functions similarly as the horizontal. With an NTSC composite sync signal the VDP vertically syncs to the last of the 6 vertical pulses. The trailing equalizing pulses act as horizontal sync pulses to the VDP. This timing chain causes the VDP to be interlaced which is different from its normal non-interlaced operation.

Some of the difficulties encountered in the timing control of the VDP relate to the other parts of its operation. It is responsible for refreshing the dynamic ram that serves as its display memory. The VDP must reset to within a pixel. There are 2 pixels for each ram memory access, which requires the termination of the half memory cycle that may be created.

The bias circuit is necessary to match the external video luma and chroma values to the VDP's luma and chroma. In Figure 1 it is seen that the internal

video from the resistor taps must finally pass through a source follower transistor. This lowers the level output by one MOS threshhold voltage typically .7 volt. So it is necessary to AC and DC bias the input external video signal to make the colors appear with the visually desired effect.

A limitation exists in the resolution of the VDP's generated image that is commonly found in low cost video mixing circuits. It still allows a display that is quite readable and useful. In the NTSC system there is an explicit relationship between the horizontal sync and the color subcarrier frequencies. The color subcarrier must be an odd multiple of one half of the horizontal sync frequency. This multiple is chosen to be 455. This is so because when the NTSC standard was set up, it was desired to have it compatible with the existing monochrome and sound subcarrier standards and to allow transmission with minimal interference between the monochrome and color signals. The relationship is :

455*horiz. sync freq/2=subcarrier freq.

Since the pixels are generated at 5.3 Mhz then:

3/2 of a VDP pixel=1/subcarrier freq.

Combining the two equations we get:

VDP pixels/ horizontal sync =455*3/4=341¼

Thus there are 341¼ VDP pixels per external horizontal line. This causes what is known as the zipper effect. On each succeeding horizontal line there is a ¼ pixel displacement of the VDP generated image. This creates a sawtooth edge surrounding all vertical edges of VDP generated images. This ¼ pixel represents a time of 47 nanoseconds, the VDP is capable of discriminating 1 pixel or 186ns.

There is no simple way to compensate for this external to the VDP without tearing signals apart and reconstructing them. A way to eliminate this internally is possible, though it is currently not implemented. This is to digitally detect the logic clock phase on which a sync pulse is first recognized and then to gate the video out on that same phase. Thus there would be a constant delay from sync to screen images.

Another way to remove the zipper would be to have two clock sources to the VDP. One clock source would be phase locked to the color subcarrier and would generate the color clocks only. The other clock source would be locked to an integer multiple of the horizontal sync and would supply the clocks to the horizontal and vertical timing sections. It should be noted that the zipper effect may be currently removed by locking the VDP's input clock to a horizontal sync integer multiple, thus maintaining a constant relationship of VDP pixel to external pixel. The colors generated from the VDP are lost however, since its color subcarrier is now out of spec of the color lock in range of a television.

It is simpler to interface two VDP's together. No sync stripper is necessary nor are any phase locked loops. The system configuration is shown in Figure 4. The VDP's run off the same crystal and are reset together. The reset signal synchronizes the internal states of each VDP to one another. Thus the two VDP's run in open loop sync. It is necessary to put VDP #2 in the external video mode to enable the mixing.

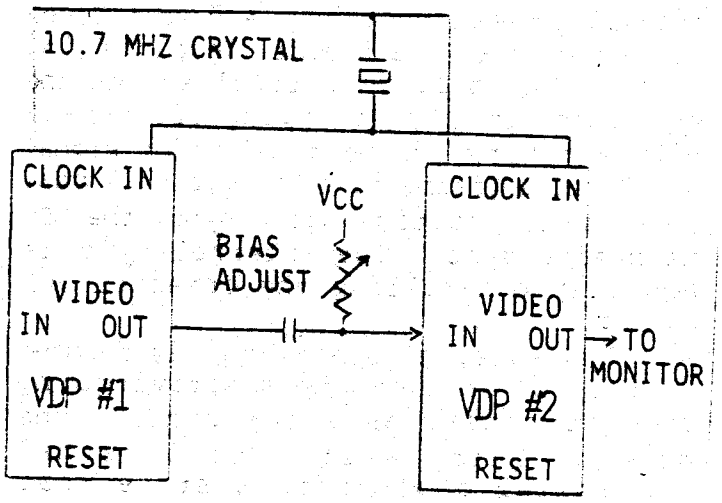


FIGURE 4 VDP TO VDP INTERFACE

By varying the bias resistor the luma relationships are changed and thus 30 different colors will be produced. By slightly shifting the clock inputs to one of the VDP's the chroma relationships are changed and thus one may choose the colors to ones liking. One may add more VDP's or even a broadcast signal to the video chain.

SOFTWARE

The software required to activate the external video feature of the VDP is rather simple. The main elements that are required are :

1. The external video enable bit must be set.

2. The background color register must be set to transparent.

3. The transparent code must be programmed at the desired screen locations.

The versatility of the transparent color can be used as any other color and thus pictures may be painted using the pallete of the external video.

CONCLUSIONS

The external video feature of a display processor is a new way to implement mixed displays in a low cost manner. The inclusion of the proper hooks for the software allows the programmer to easily display powerful images.

BIOGRAPHY

PETER H MACOUREK received his BSEE with a minor in biomedical engineering from the University of Arizona in 1975. Since 1976 he has worked as a MOS design engineer with the Microprocessor Design Department of Texas Instruments in Houston. As one of the designers of the 9918 he is a co-holder of a patent pending on the device. Mr. Macourek also specializes in the field of computer simulation and testing.