ALPHA - 9900 COMPARISON

APPROX MEMORY ACCESS TIMES (IN NANO-SECONDS)

	ALPHA @ 6 MHz (INTERNAL)			9995/16 @ 3 MHz		9900	
	NO WAIT	ONE WAIT	TWO WAITS	NO WAIT	ONE WAIT	4 MHz	3 MHz
CYCLE	167	333	500	333	666	500	666
ACCESS	85	251	417	120	450	370	490

EXAMPLE EXECUTION TIMES

MOV R,R	500	1000	1500	1000	2000	3500	4666
MOV SYM,SYM	833	1667	2500	1667	3333	7500	10000
MOV *R+,*R+	1500	2667	3834	3000	5333	7500	10000
ADD R,R	667	1333	2000	1333	2667	3500	4666
ADD SYM,R	833	1667	2500	1667	3333	5500	7333
JUMP REL.	500	667	833	1000	1333	2500	3333
MPY R,R	4000	4833	5667	8000	9666	13000	17316
DIV R,R	5166	6166	7166	10333	12333	27000	35964
						(AVG)	(AVG)

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ALPHA - COMPITITIONS COMPARISON

APPROX MEMORY ACCESS TIMES (IN NANO-SECONDS)

	ALPHA @ 6 MHz (INTERNAL) NO WAIT	ONE WAIT	TWO WAITS	68000 @ 4 MHz	8086 o @ 8 MHz	Z8000 @ 4 MHz
CYCLE	167	333	500	500	500	750
ACCESS	85	251	417	280	290	400
ACCESS/CYCLE	50%	75%	83%	53%	58%	53%

EXAMPLE EXECUTION TIMES

MOV R,R	500	1000	1500	500	375	750
MOV SYM,SYM	833	1667	2500	2500	3125 T	5000 T
MOV *R+,*R+	1500	2667	3834	1500	2125	5000
ADD R,R	667	1333	2000	500	375	1000
ADD SYM,R	833	1667	2500	1500	1875	2250
JUMP REL.	500	667	833	1250	2000	1500
MPY R,R	4000	4833	5667	8750	18000	17500
DIV R,R	5166	6166	7166	19750	22125	23750

T REQUIRES TWO INSTRUCTIONS

o 8086 TIMES DO NOT INCLUDE POSSIBLE QUE MAINTENANCE PROBLEMS EXCEPT FOR JUMP RELATIVE WHICH ACCOUNTS FOR QUE FLUSHING

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FIGURE 4

SOME KEY INSTRUCTION COMPARISONS

(ALPHA GIVEN AS ONE WAIT FOR NON REG AND (ONE)/(NONE) FOR REG. ACCESS AND ONE WAIT STATE FOR ALL OTHER ACCESSES)

	ALPHA @ 8 MHz	68000 @ 8 MHz	8086 @ 6 MHz	Z8000 @ 8 MHz	9900 @ 4 MHz
ADD R, R	2000/1250 S	500 S	429 S	800 S	3500
ADD SYMB, R	2500/2000 S	1500 S	2006	1800	5500
ADD R, SYMB	2500/2250 S	2000 S	3000	3800 B	5500
MPYS R, R	7750/6750	8750	20571	14000	13000 U
DIVS R, R	10000/9000	19750	25286	19000	27000 U
JUMP RELATIVE	1000/1000	1250	2286	1200	2500
MOVE *R+, *R+	4000/3000	1500 S	2429	4000	7500
MOVE SYMB, SYMB	2500/2500 S	2500 S	3571 B	4000	7500

S = SOLID MEMORY CYCLES (I.E., MEMORY ACCESS LIMITED)
B = REQUIRES 2 INSTRUCTIONS
NOTE COMPARISON DOES NOT INCLUDE ADDRESS MODES THAT THE ALPHA DOES NOT SUPPORT BUT THAT THE OTHERS DO (I.E., THIS COMPARISON TENDS TO FAVOR OF ALPHA SINCE IT IS DONE FROM THE 9900 SET POINT OF VIEW)
U = UNSIGNED

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9900 – 99000 Execution Comparison

Example ADD R,R followed by JMP

9900

STATE	MEMORY	INTERNAL
A1	IF	
A2	—	DECODE & WP+2S
A3	SF	
A4	—	WP+2D
A5	DF	
A6	—	Execute ADD
A7	DW	
J1	IF	DECODE & WP+2S
J2	—	
J3	—	
J4	—	PC + DISP
J5	—	
	IF	

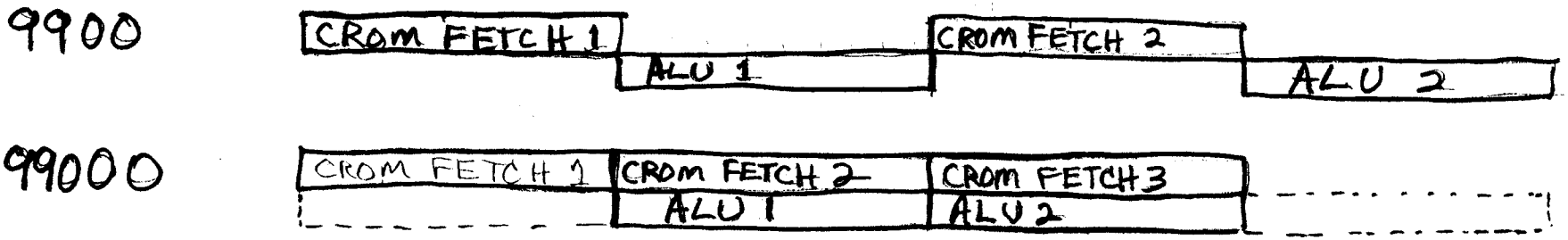
TOTAL 12 STATES @ 2 Clock CYCLE/STATE
333 NS/CLOCK ⇒ 8 µS

99000

STATE	MEMORY	INTERNAL
A1	IF	
	Prev. DW	Decode & WP+2S
A2	SF	WP+2D
A3	DF	Source → T
J1	IF	Execute ADD
A4	DW	Decode JMP
J2	—	PC+DISP
	IF	
J3	—	

TOTAL 7 STATES @ 1 CLOCK/STATE
166 NS/CLOCK ⇒ 1.166 µS

CROM EXECUTION



SYTEM and Logic Design Results in about a 3.5X improvement in speed Assuming the same ALU performance.
(With the 99000's 2X clock speed of 6 mhz/state this gives 7X 3MHZ 9900)

ALPHA INSTRUCTION AND FEATURE ADDITIONS

- * - 16 BIT SIGNED MULTIPLY AND DIVIDE
- \- 32 BIT ADD SUB, SHIFT LEFT AND SHIFT RIGHT
- * - LOAD WORKSPACE AND LOAD STATUS FROM REGISTER
- \- BIT MANIPULATION - MULTIPROCESSOR TEST, TEST AND SET, TEST AND CLEAR
- \- BRANCH AND PUSH LINK, BRANCH INDIRECT
- \- ARITHMETIC OVERFLOW TRAP
- \- PRIVELEDGED MODE
- \- MEMORY MAPPER CONTROL INSTRUCTIONS
- \- PARALLEL I/O INTERFACE SEPARATE FROM MEMORY SPACE
- \- BUS STATUS SIGNALS TO INDICATE PROCESSOR ACTIVITY
- \- EXTERNAL PROCESSOR INTERFACE
- * - CRYSTAL OSCILLATOR INPUTS
- \- PAGE AND/OR MEMORY MAPPER CONTROL OUTPUT
- * - SINGLE 5 VOLT SUPPLY
- * - 40 PIN PACKAGE

* IMPLEMENTED ON 9985A

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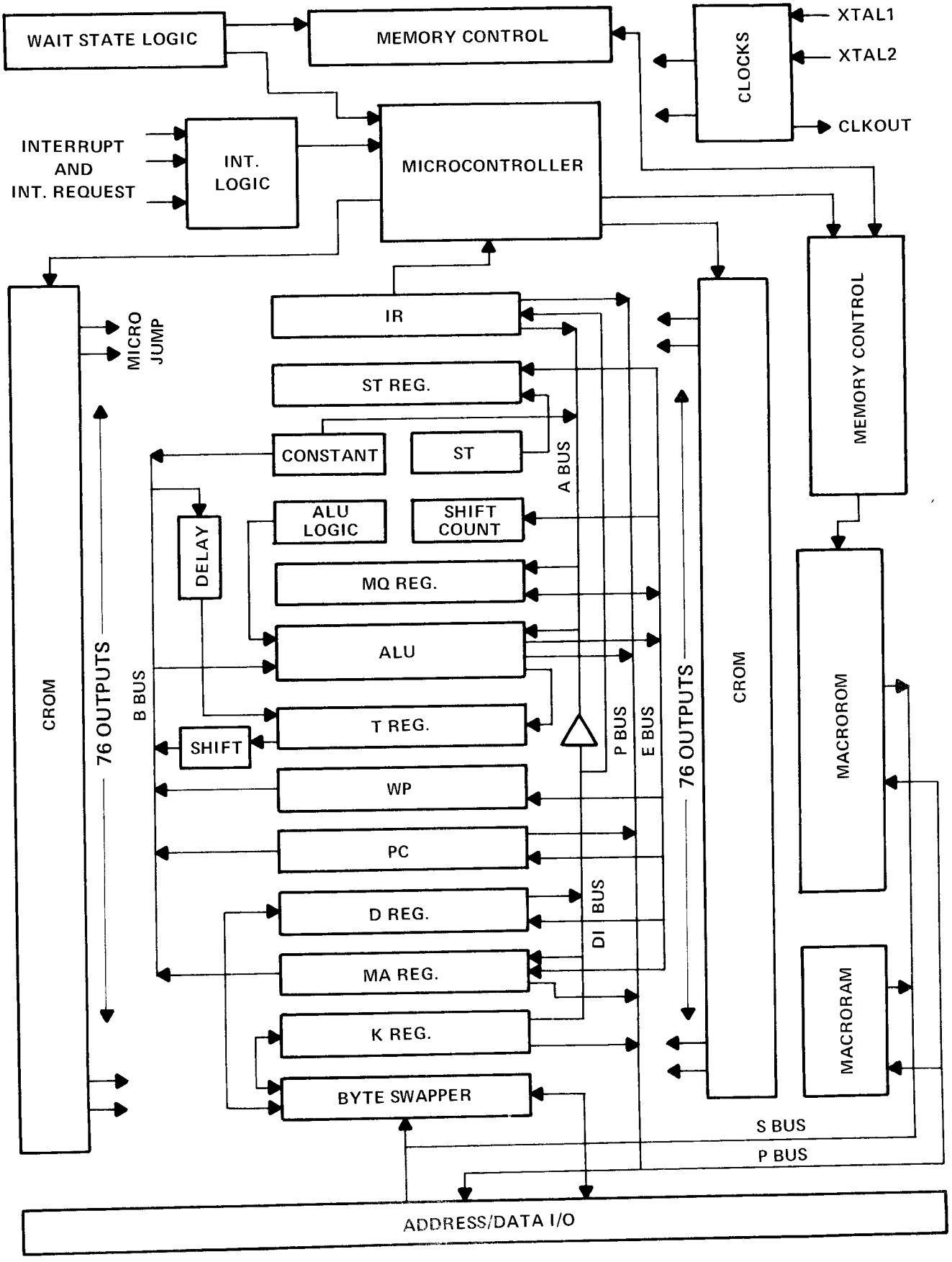
WAIT STATE LOGIC
MEMORY CONTROL
CLOCKS
XTAL1
XTAL2
CLKOUT
INTERRUPT AND INT. REQUEST
INT. LOGIC
MICROCONTROLLER
MEMORY CONTROL
IR
MICRO JUMP
ST REG.
CONSTANT
ST
A BUS
ALU LOGIC
SHIFT COUNT
DELAY
MQ REG.
ALU
CROM
76 OUTPUTS
B BUS
T REG.
SHIFT
P BUS
E BUS
WP
PC
D REG.
DI BUS
MA REG.
K REG.
BYTE SWAPPER
CROM
MACROROM
MACRORAM
S BUS
P BUS
ADDRESS/DATA I/O

CONCLUSIONS ON PERFORMANCE

1. THE ALPHA IS PERFORMANCE COMPETITIVE WITH THE 8086 AND Z8000. POTENTIAL PROBLEM AREAS ARE THE LACK OF BLOCK INSTRUCTIONS, FEWER ADDRESSING MODES, AND MEMORY MAPPING SCHEME. ALSO THE 8086 AND Z8000 COULD BE REDESIGNED TO HAVE BETTER PERFORMANCE.

2. THE 68000 HAS ABOUT TWICE THE PERFORMANCE OF ALPHA ON GENERAL PURPOSE BENCHMARKS WITH EQUIVALENT MEMORY SYSTEMS. ALPHA CAN NARROW THIS GAP WITH BETTER MEMORY SYSTEMS. THE PERFORMANCE DIFFERENCES ARE DUE TO THE WORKSPACE CONCEPT AND A LESSER INSTRUCTION SET. THE 68000 HAS BEEN POORLY DESIGNED, IN THAT IT WASTES BAR AREA; IT SHOULD BE EXPECTED THAT THE RELAYOUTS AND REDESIGN WILL REDUCE THESE PROBLEMS, THUS MAKING THE 68000 COMMERCIALLY PRACTICAL. ALSO INTEL IS EXPECTED TO ANNOUNCE A "32" BIT PROCESSOR SOON.

3. ALPHA WILL HAVE TO BEAT ITS COMPETITORS ON SUPPORT, AVAILABILITY, COST, AND MARKETING. IN SOME APPLICATIONS IT WILL BEAT THE OTHERS ON PERFORMANCE.

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FIGURE 3

APPROX. MEM ACCESS TIMES
(IN NANO SEC)

	ALPHA @ 4 MHz (INTERNAL)[1]		68000 @ 8 MHz	8086 @ 6 MHz	Z8000 @ 4.3 MHz	9900 @ 4 MHz
	ONE WAIT	NO WAIT				
CYCLE	500	250	500	666	697	500
ACCESS	380	130	380[2]	380[3]	380[4]	370
ACCESS/ CYCLE	76%	48%	76%	58%	53%	76%

1) EXTERNAL CRYSTAL FREQUENCY WILL BE EITHER 2 TIMES OR 4 TIMES THE INTERNAL FREQUENCY

2) BASED ON DATA OBTAINED BY SYSTEM DEVELOPMENT CORP.

3) PRO-RATED FROM 5 MHZ AND 8 MHz DATA

4) PRO-RATED FROM 4 MHz AND 6 MHz DATA

* ABOVE DATA IS INTENDED TO NORMALIZE ALL PROCESSORS TO ABOUT THE SAME MEMORY ACCESS TIME, FOR USE IN THE KEY INSTRUCTION COMPARISONS TO FOLLOW. NOTE THAT ALL ABOVE PROCESSORS ARE PROJECTED TO RUN FASTER THAN SPECIFIED ABOVE.

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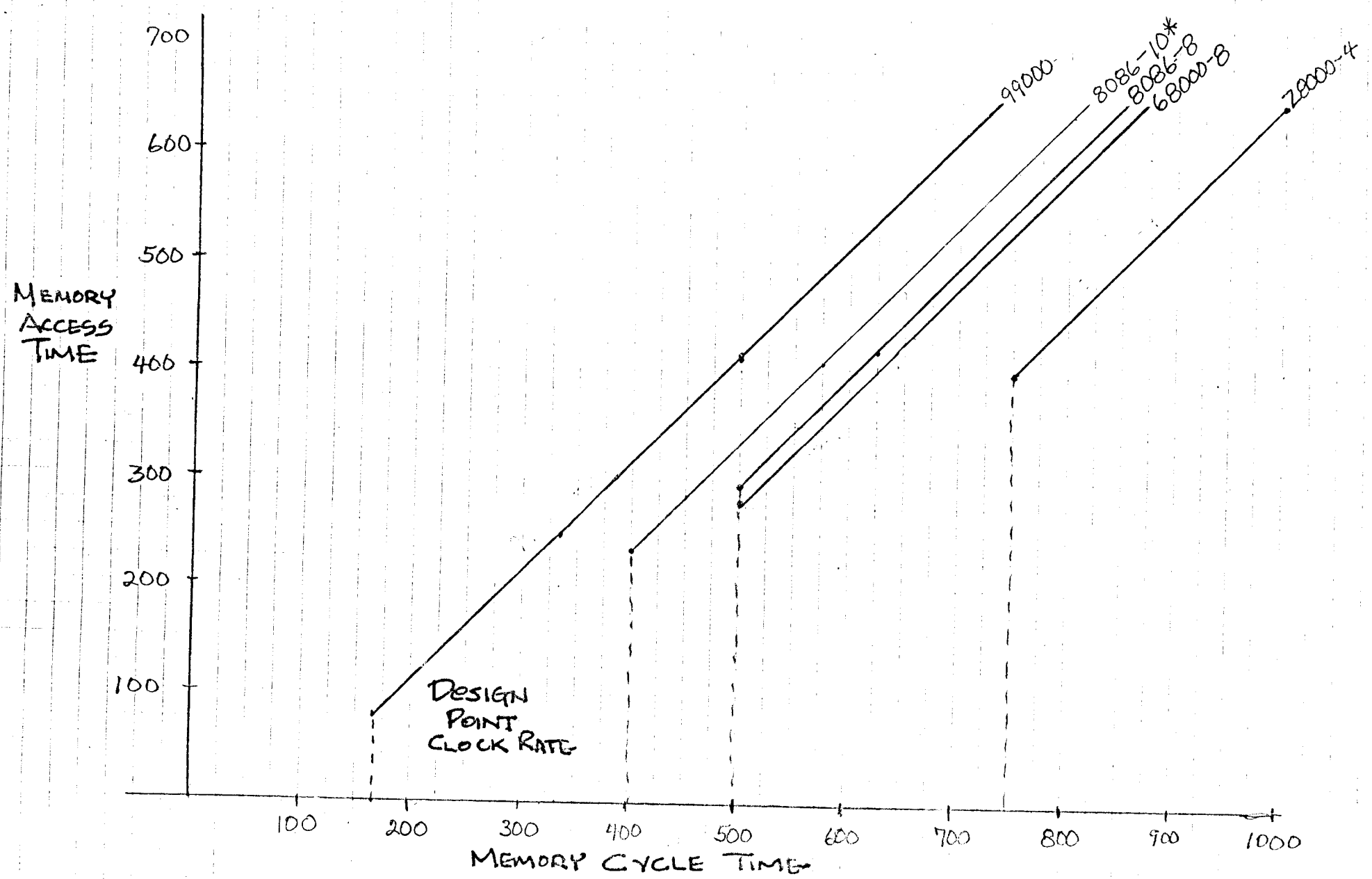
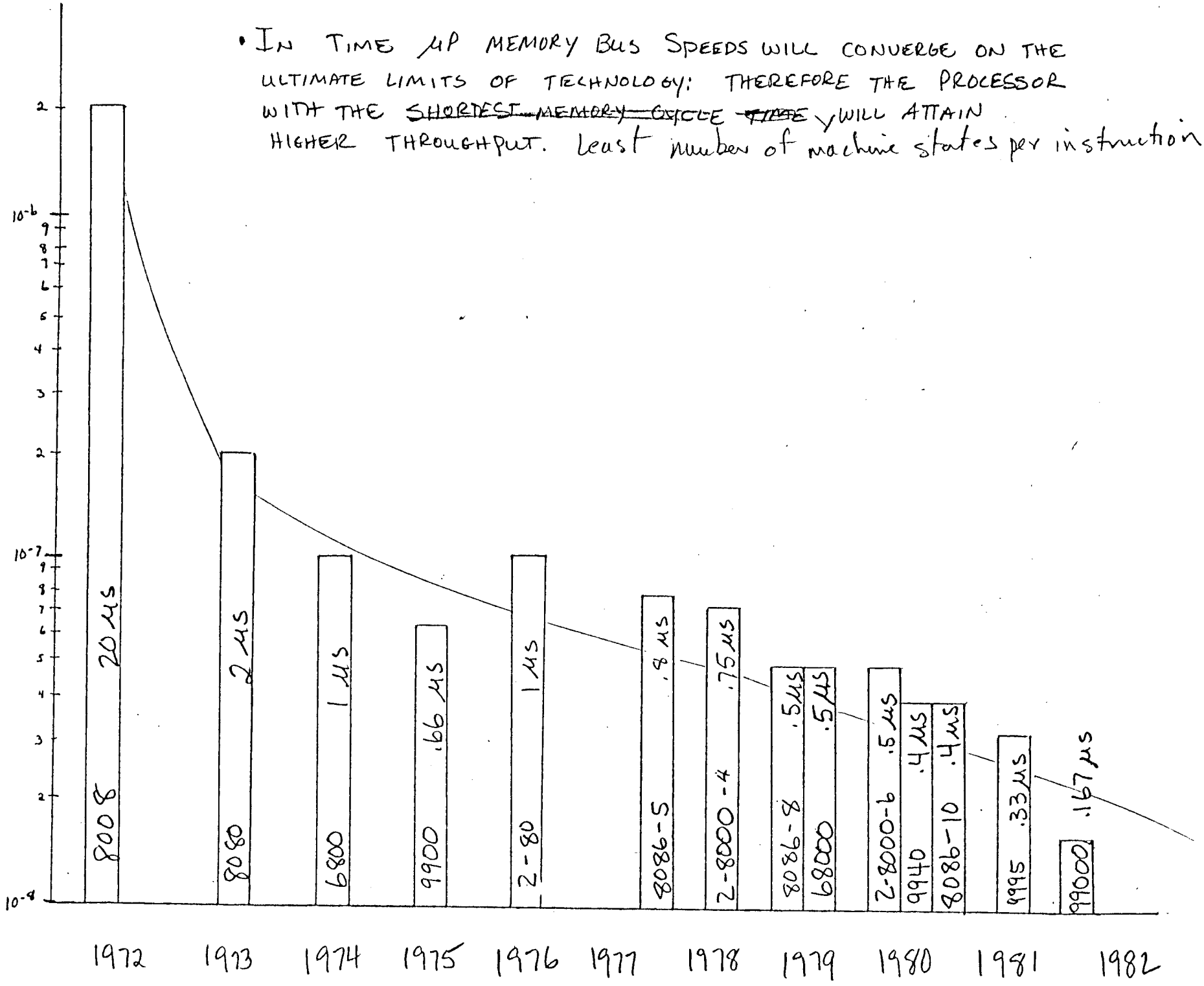
990/10 "TYPICAL" INSTRUCTION MIX
(ALL NUMBERS IN PERCENTS (%))

	PERCENT USAGE ON 990/10	99000 OPCODE SPACE	68000 OPCODE SPACE
MOV (23.1), MOVB (7.1)	30.2	12.5	25.0
JUMPS, SBD, SBZ, TB	21.5	6.3	6.5
INC, DEC, INV, NEG, CLR, X, SWPB, SETO, ABS	12.5	.9	9.4
AI, LI, CI, ANDI, ORI	9.1	.1	5.0
A, S, C, SZC, SOC	7.4	62.5	2.5
B	6.8	.1	.1
SHIFTS	4.0	1.6	7.0
BL (MINOR SUBROUTINE)	3.8	.1	.1
LDS LDD	1.9	.2	-
RTWP (SUBROUTINE RETURN)	.8	.002	.005
BLWP (MAJOR SUBROUTINE)	.43	.1	.1
OTHERS	2.0	13.1	
ILLEGAL	-	2.5	21.9



* 8086-10 is a projection from the 8086-8

• In time µP memory bus speeds will converge on the ultimate limits of technology; therefore the processor with the ~~shortest memory cycle time~~ will attain higher throughput. least number of machine states per instruction



1943 - Hardvard Mark 1 (relay type) funded by IBM under Prof. Aiken
1943 - Colossus (elec. tube code breaking computer) - Great Britain
1945 - "First Draft of a Report on the EDVAC" by Von Neuman
1946 - ENIAC at Moore School of Engr. (U of Penn.) under Eckert and Mauchly
(with key help from Von Neuman and Goldstine)
1947 - Transitor (point contact germanium) at Bell by Barden, Brattain, &
Shockley
1948 - Machester Mark 1 (First Operational Stored Program Computer) - G.B.
1948 - Selective Sequencial Electronic Calculator (SSEC) by IBM
1951 - MIT Whirlwind functional under Forrester
1951 - Univac Functional
1953 - Magnetic Core memory used in Whirlwind at MIT
1954 - Practical Silicon Transistor at Texas Instruments by Teal
1957 - FORTRAN at IBM by Backus and Ziller
1958 - Planar Transistor by Fairchild
1959 - First Integrated Circuit at Texas Instruments by Kilby
1959 - PDP-1 at DEC (cost about $120K)
1961 - STRETCH built at IBM ("No market for large computers")
1962 - 16 MOS transitor I.C. by RCA
1965 - IBM 360 ($500M in R&D)
1965 - PDP-8 First "Off the shelf" computer and under $20K
1970 - PDP-11 at DEC
1970 - IBM 370