SONY V7021

NTSC/PAL Decoder

T-77-29

Description

V7021 is a decoder IC used to convert composite video signals into analog RGB signals. It has signal outputs, such as composite sync, burst flag, sub-carrier, and alternate signal outputs, necessary for image processing. V7021 operates in both NTSC and PAL mode.

Features

- 5V single supply operation
- Low power consumption (about 85mW)
- Compatible with both NTSC and PAL modes.
- Provides composite sync, burst flag, sub-carrier, and line alternate signal outputs.

Function

Synchronous separation, Composite sync output, burst flag output, ACC, ACK, APC, demodulator, Y/C mixer, DL amplifier, PAL ID, HUE control

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings

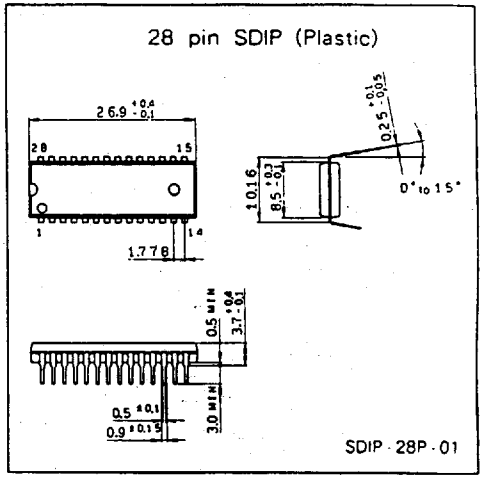
• Supply voltage	V_{CC}	10	V
• Operating temperature	Topr	−20 to +75	℃
• Storage temperature	Tstg	−55 to +150	℃
• Allowable power dissipation	P_D	1250	mW

Recommended Operating Conditions

• Supply voltage	V_{CC}	5 ± 0.25	V

Package Outline

Unit : mm



8/91 version

81118 - ST

Block Diagram and Pin Configuration

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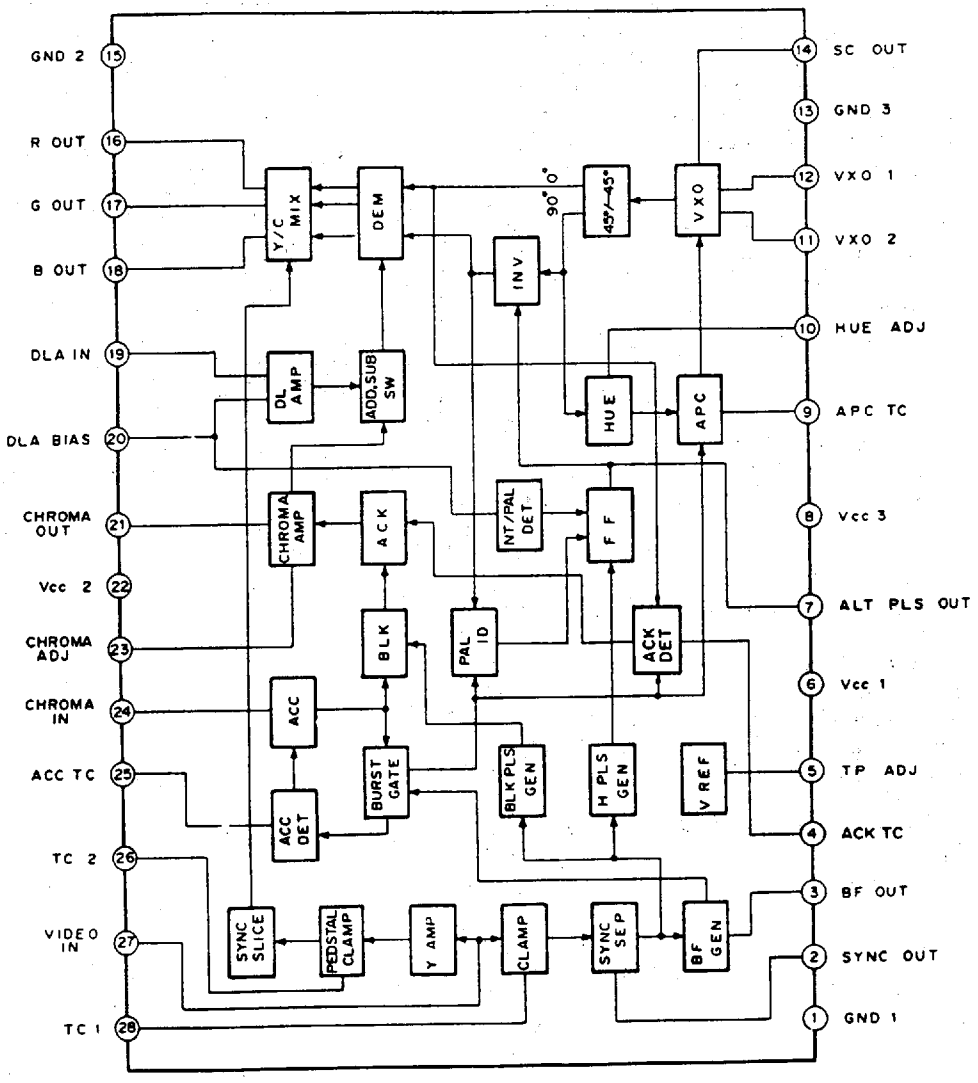

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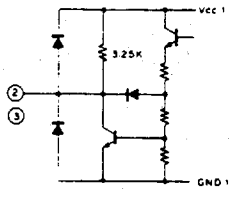
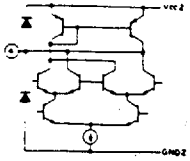
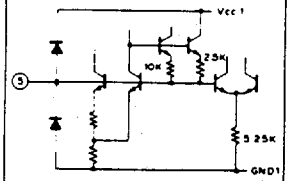
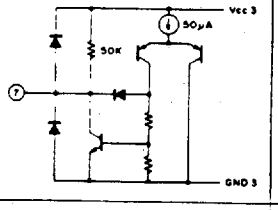
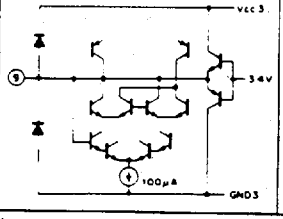
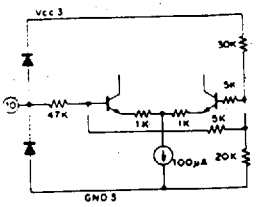
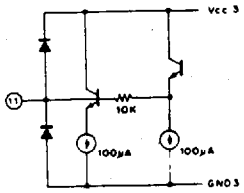
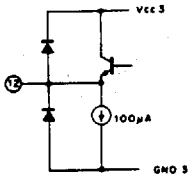
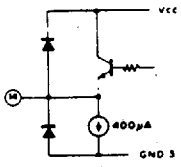
Pin Description

No.	Symbol	Voltage	Equivalent circuit	Description
1	GND 1	0V		GND pin of Y AMP and SYNC SEP.
2	SYNC OUT	H ; 2.4V Min. L ; 0.4V Max.		Composite sync output pin (TTL level)
3	BF OUT			Burst flag output pin (TTL level)
4	ACK TC	3.1V Typ.		ACK (Auto Color Killer) time constant pin
5	TP ADJ	1.23V Typ.		Burst flag positional adjusting pin By changing the current from this pin burst flag position adjustment to tD (BF) = 5.6 µs can be performed.
6	Vcc 1	5V*		Supply pin of Y AMP and SYNC SEP.
7	ALT PLS OUT	H ; 2.4V Min. L ; 0.4V Max.		Line alternate pulse output pin NTSC mode ; L PAL mode ; Alternate H and L every 1H.
8	Vcc 3	5V*		Supply pin of APC, HUE, VXO and SYNC SEP.
9	APC TC	3.4V*		APC (Auto Phase Control) time constant and fo adjusting pin By varying the DC voltage to be applied to this pin, free running frequency of VXO adjustment can be performed.

* **Note)** External apply voltage.

No.	Symbol	Voltage	Equivalent circuit	Description
10	HUE ADJ	2.0V *		Pin for adjusting HUE. By applying 0 to 5V to this pin, more than ±30° HUE can be adjusted. When in PAL mode, it is grounded by the capacitor.
11	VXO2	3.1V (Typ.)		Pin for crystal oscillator.
12	VXO1	3.3V (Typ.)		Pin for crystal oscillator.
13	GND3	0V		Ground pin for APC, HUE, and VXO
14	SC OUT	1.8V (Typ.)		Sub-carrier output pin
15	GND2	0V		Ground pin for demodulator and Y/C mixer.

* **Note**) External apply voltage.

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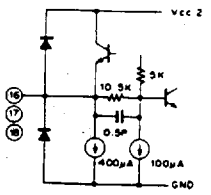
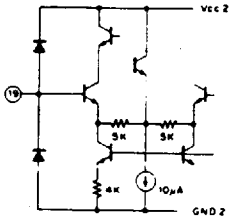
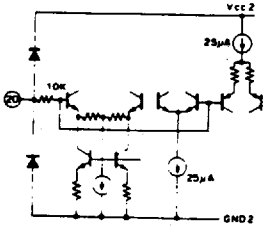
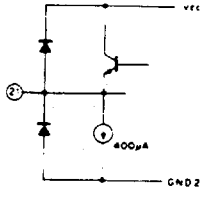
No.	Symbol	Voltage	Equivalent circuit	Description
16	R OUT	2.0V (Typ.)		R output pin
17	G OUT			G output pin
18	B OUT			B output pin
19	DLA IN	2.3V* (PAL) 0V* (NTSC)		DL amplifier input pin. This must be grounded in NTSC mode. The 1HDL output must be connected in PAL mode.
20	DLA BIAS	2.3V* (PAL) 0V* (NTSC)		Selects NTSC or PAL mode, and adjusts DL amplifier again in PAL mode NTSC mode : V_{20} 0.8V max. PAL mode : V_{20} 1.8V min. 2.8V max. The variable range is ± 3dB min.
21	CHROMA OUT	3.7V (Typ.)		Chroma output pin. It is connected to V_{CC2} in NTSC mode, and to the 1HDL input in PAL mode.
22	V_{CC2}	5V		Power pin of demodulator and Y/C mixer.

* **Note**) External apply voltage.

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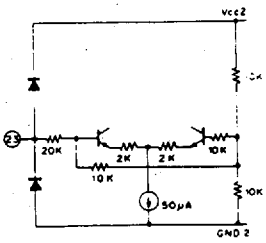
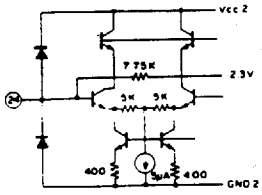
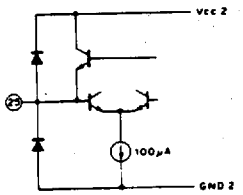
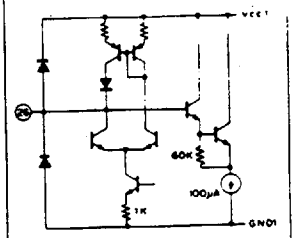
No.	Symbol	Voltage	Equivalent circuit	Description
23	CHROMA ADJ	2.5V (Typ.)		The voltage applied to this pin selects monochrome (BW) or color mode. Monochrome mode : V23 0.8V max. Color mode : V23 2.0V min. 3.0V max. The variable range is – 20dB to more than 0dB.
24	CHROMA IN	2.3V (Typ.)		Chroma signal input pin. The standard input level is burst amplitude 143mVp-p.
25	ACC TC			Pin for ACC time constant.
26	TC2			Pin for pedestal clamp time constant.

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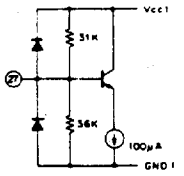
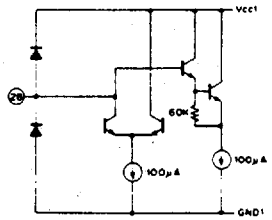
No.	Symbol	Voltage	Equivalent circuit	Description
27	VIDEO IN	2.7V (Typ.)		Input pin of video signal (luminance and SYNC). The standard input level is 0.36Vp-p.
28	TC1			Pin for feedback clamp time constant for SYNC SEP.

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Electrical Characteristics (Vcc = 5V Ta = 25°C See the Electrical Characteristic Test Circuit.)

Item		Symbol	Conditions	Input signal V	Input signal C	Test point	Min.	Typ.	Max.	Unit
Supply current 1		ICC1	Signal for no chroma input	2	–	6	3.45	4.55	6.70	mA
Supply current 2		ICC2	PAL mode			22	5.48	7.24	10.65	mA
Supply current 3		ICC3				8	3.13	4.13	6.07	mA
Video amplifier voltage gain		VO(R)	VAC = 0.1Vp-p f = 100kHz VDC = 0.125V See test method 1 for details	1	–	16	10.8	11.8	12.8	dB
		VO(G)				17				
		VO(B)				18				
Video amplifier 3-dB bandwidth		fC(R)	Input frequency which becomes −3dB when 100kHz output is 0dB.	1	–	16	5.0			MHz
		fC(G)				17				
		fC(B)				18				
Video amplifier maximum output		VOM(R)	VAC = 0.32Vp-p f = 100kHz VDC = 0.16V	1	–	16	1.1			Vp-p
		VOM(G)				17				
		VOM(B)				18				
Demodulation output DC voltage		EODC(R)	Signal for no chroma input	2	–	16	1.4	2.0	2.8	V
		EODC(G)				17				
		EODC(B)				18				
Original color output voltage		EO(R)	See test method 2 for details	3	5/7	16	0.9	1.0	1.1	Vp-p
		EO(G)				17				
		EO(B)				18				
Demodulation output residual carrier		CL(R)	Signal for no chroma input 3.58MHz component	2	–	16			40	mVp-p
		CL(G)				17				
		CL(B)				18				
ACC characteristic 1		ACC1	$ACC1 = \frac{Voc\ (Vin = -14dB)}{Voc\ (Vin = 0dB)}$	3	5/7	21	−3.0	−1.0		dB
ACC characteristic 2		ACC2	$ACC2 = \frac{Voc\ (Vin = +6dB)}{Voc\ (Vin = 0dB)}$	3	5/7	21		+1.0	+3.0	dB
Color killer level		ek	Chroma input level during color killer operation	3	5/7	24	−44	−38	−32	dB
APC lock in range		fp		2	6/8	14	±300			Hz
Sync output	H	VOH(S)		2	–	2	2.4			V
	L	VOL(S)							0.4	V
	Delay	tD(S)					0.4	0.5	0.6	µs
Burst flag output	H	VOH(BF)		2	–	3	2.4			V
	L	VOL(BF)		2	–	3			0.4	V
	Pulse width	tW(BF)	When adjusted to tD (BF) = 5.6 µs	2	–	3	2.2	2.4	2.6	µs
Blanking pulse width		tW(BLK)		2	4	18	9.0	10.0	11.0	µs
Sub-carrier output		VO(SC)		3	5/7	14	400	500		mVp-p
Alternate pulse output	H	VOH(ALT)	PAL mode	3	5/7	7	2.4			V
	L	VOL(ALT)							0.4	

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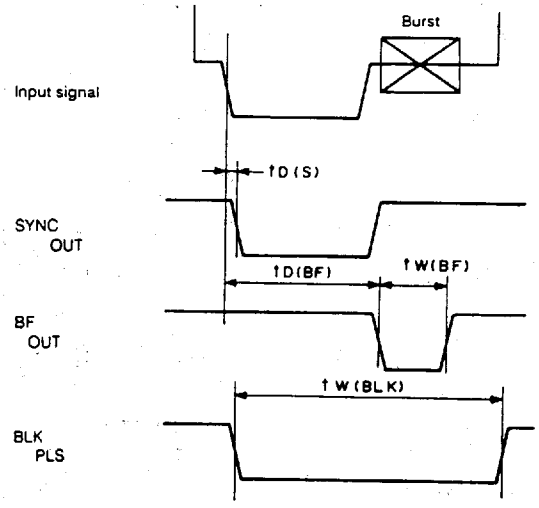
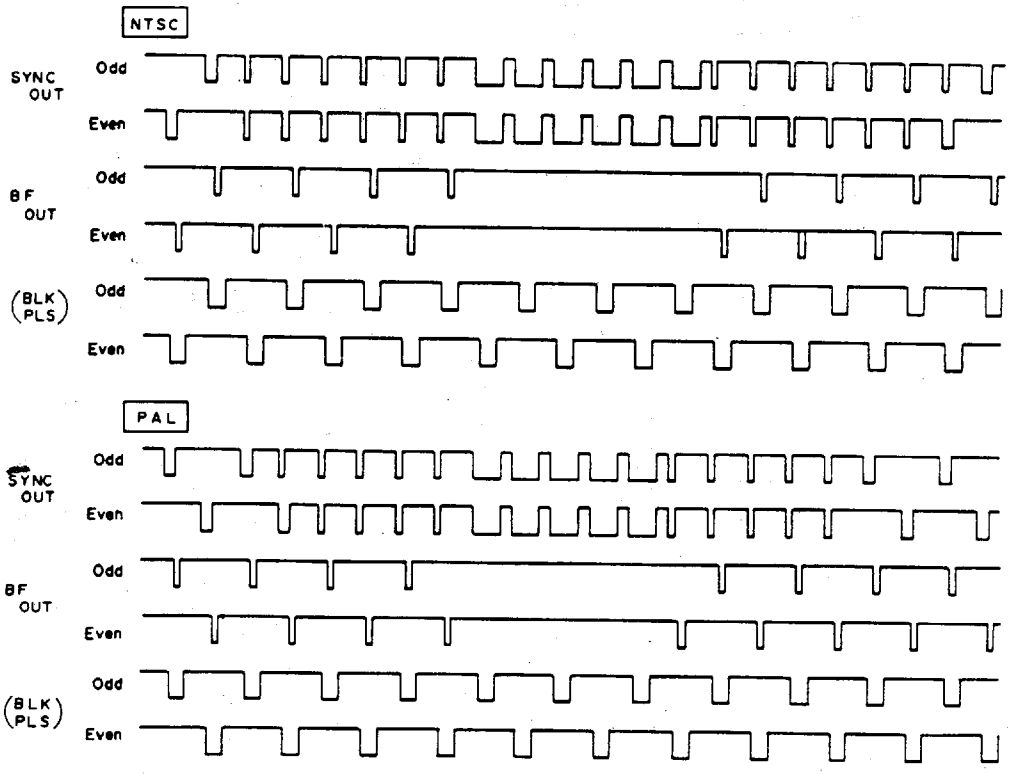
Synchronization System Timing Chart

H SYNC



V. SYNC



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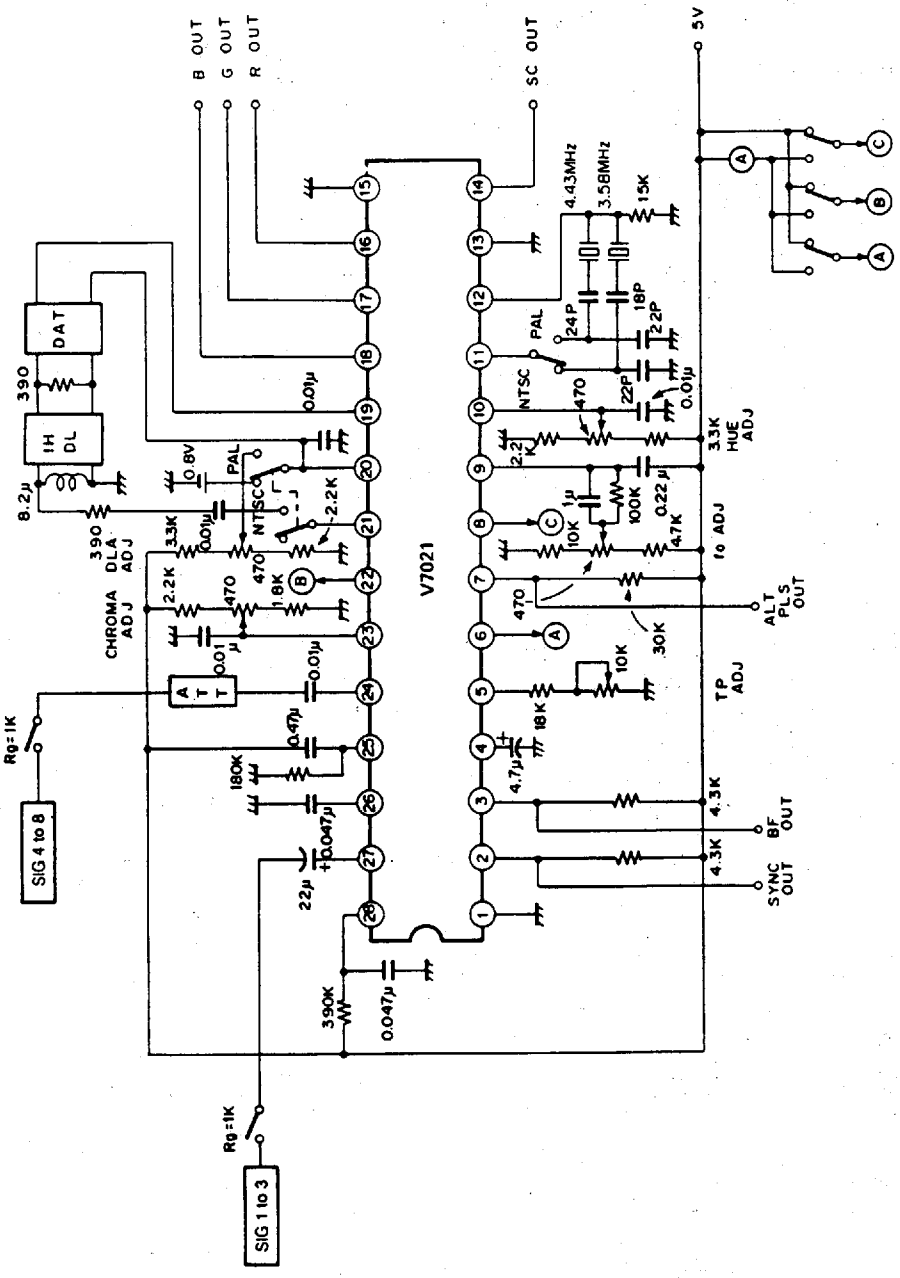
Electrical Characteristics Test Circuit



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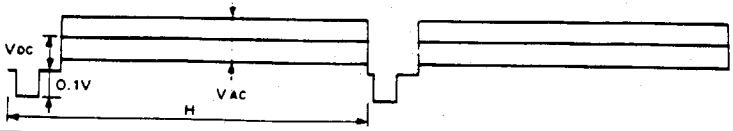
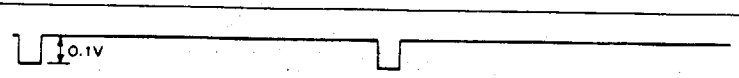
Input signal

V

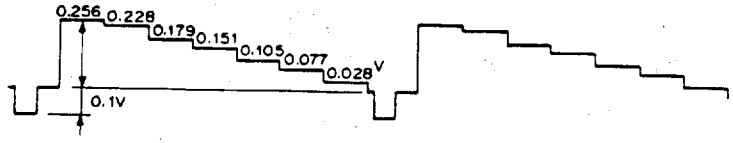
SIG 1



SIG 2



SIG 3

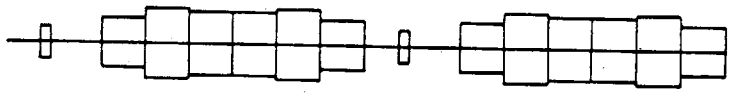


C

SIG 4

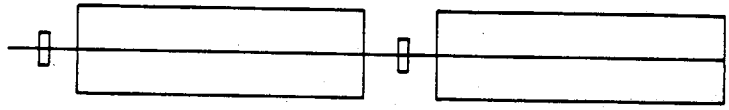
Sine wave Frequency 3.579545MHz
Amplitude 143mVp-p

SIG 5



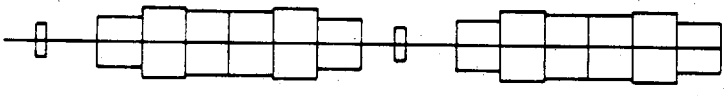
Amplitude	143	320	451	422	422	451	320	mVp-p
Phase	180	168	284	241	61	104	348	deg
Frequency		3.579545 MHz						

SIG 6



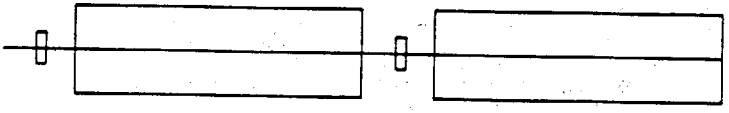
Amplitude	143	436	mVp-p
Phase	180	0	deg
Frequency		3.579545 MHz	±300 Hz

SIG 7



Amplitude	143	320	451	422	422	451	320	143	320	451	422	422	451	320	mVp-p
Phase	135	168	284	241	61	104	348	225	192	76	119	299	256	12	deg
Frequency		4.433619 MHz													

SIG 8



Amplitude	143	436	143	436	mVp-p
Phase	135	0	225	0	deg
Frequency		4.433619 MHz	±300 Hz		

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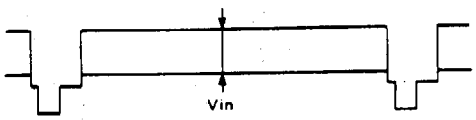
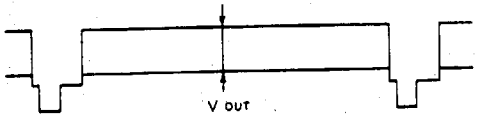
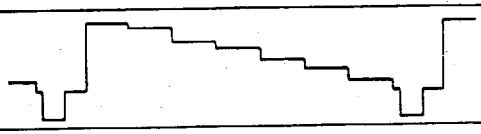
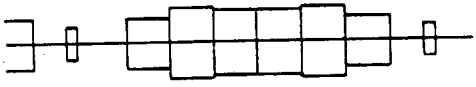
Test Method

1. Video amplifier voltage gain

Input waveform	VIDEO IN	
	CHROMA IN	Non-signal input
Output waveform	R G OUT B	

$$Gv = 20\log\frac{Vout}{Vin}\ (dB)$$

2. Original color output voltage

Input waveform	VIDEO IN	
	CHROMA IN	
Output waveform	R OUT	
	G OUT	
	B OUT	

Adjustment

1. Adjust HUE ADJ so that output B is the same amplitude.
2. Adjust CHROMA ADJ so that output B is 1Vp-p.

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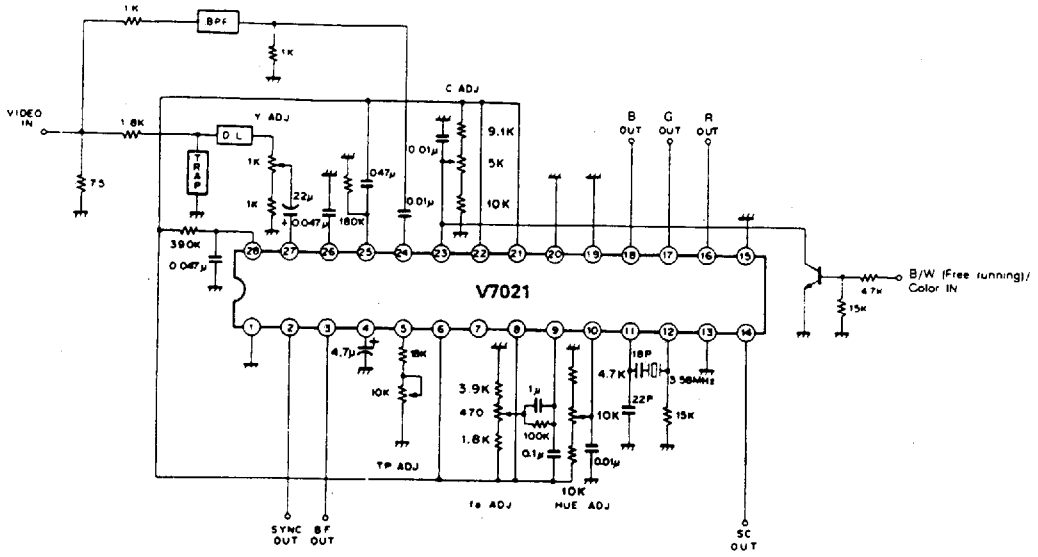
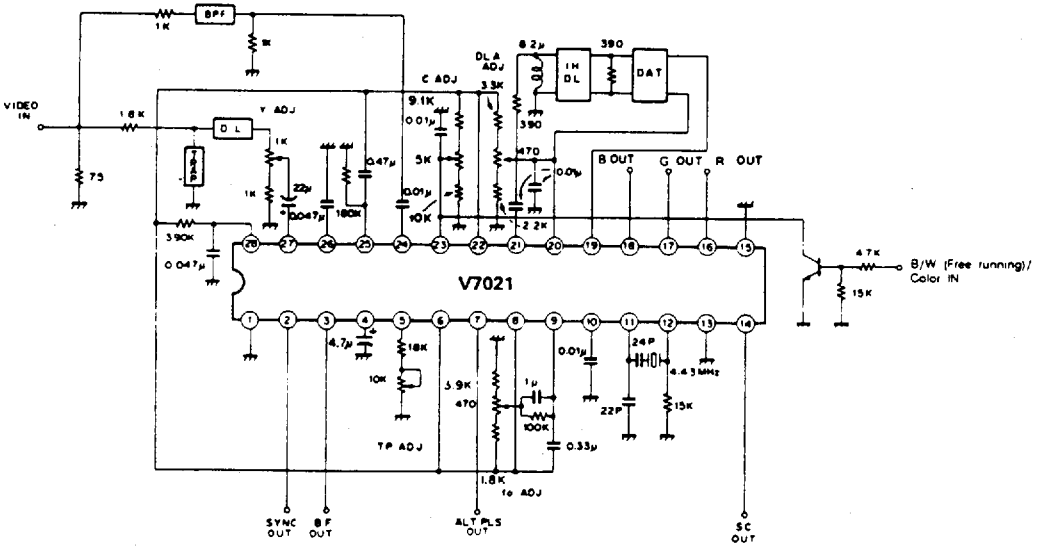
Application Circuit (NTSC mode)

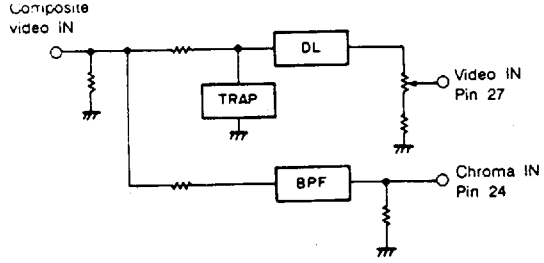


(PAL mode)



Applications

1. Input signals
Composite video signal input is separated into video signal (Y) and chroma signal (C) by band-pass filter, trap and delay line, Y is input to pin 27 and C to pin 24. While composite video signal is input at 1Vp-p, the typical levels of the input signals are as shown in the table below.



Composite video input (Synchronous negative polarity)		1.0Vp-p
Video input	Luminance	0.256Vp-p
	Sync	0.103Vp-p
Chroma input	Burst	0.143Vp-p

2. Time pulse adjustment
BF (Burst Flag) pulse positional adjustment can be performed by changing the current to be taken out from pin 5. Setting to (BF) at 5.6 µs by this adjustment results in that BF pulse width is set at approx. 2.4 µs and BLK (blanking) pulse width at 10 µs.

3. Monochrome (free-running) /color mode switching
If pin 23 (CHROMA ADJ) is set to H (≧2.0V), the color mode is established. Input chroma signal will be decoded and output in the form of color difference signal. If pin 23 is set to L (≦0.8V), the monochrome (free-running) mode is established and the APC circuit is made to stop. As a result, VXO oscillates in the free-running mode.

4. NTSC/PAL mode switching
Setting pin 20 (DL A BIAS) to H (≧2.0V), establishes the PAL mode, and setting the pin to L (≦0.8V).

5. Chroma output
Chroma signal subjected to ACC and blanking is output at pin 21 (CHROMA OUT). Output amplitude is approx. 160mVp-p with typical input (75% color bar).
In the PAL mode, this output is to be input to 1 H DL. In the NTSC mode, connect pin 21 to the power supply (Vcc).

6. DL (Delay Line) AMP
An amplifier for insertion of 1 H DL and matching loss compensation when in the PAL mode. Its gain is variable within 14 ± 4dB to absorb DL dispersion.
Its input pin is pin 19 (DL A IN) ; apply to this pin a bias voltage of the same potential as with pin 20 (DL A BIAS). The signal having passed through 1 H DL is to be input to pin 19 after adjusted at the delay adjusting transformer (DAT) so that the delay time is 1 H (64 µs).

In the NTSC mode, this amplifier is not used ; set the levels of pins 19 and 20 at L (≦0.8V).

7. VXO, APC

Pin 9 (APC TC) is the APC time constant pin. When APC circuit is not active in PC mode, free run frequency is determined by means of the DC voltage of this pin to compensate the free run frequency temperature characteristics execute temperature compensation as in the example for application circuits. VXO can be used to handle NTSC and PAL by changing the crystal oscillator and the linear capacitance.

8. Order of adjustment

Input signal 100% Color bar

[NTSC mode]

1) BF (burst flag) position adjustment
   Adjusting the resistance between pin 5 and the ground, BF position is rendered $t_D = 5.6$ µs.
2) Adjustment of video amplifier level
   Adjust YADJ with RGB output, so that white peak (100% white) becomes 1.0Vp-p.
3) f_0 adjustment
   Adjustment f_0 ADJ, so that in PC mode oscillating frequency (subcarrier output) becomes fsc.
4) HUE adjustment
   Adjust HUE ADJ so that in S1 mode, the amplitude be the same for the respective colors from B output amplitude.
5) Chroma level adjustment
   Adjust C ADJ so that the respective colours of B output amplitude, become 0.75Vp-p.

[PAL mode]

1) BF position adjustment
2) Adjustment of video amplifier level
3) f_0 adjustment.

} The same as for NTSC

4) DL amplifier adjustment.
   Adjust DLA ADJ so that in SI mode, the R output amplitude former and latter parts, in H section, be equal.
5) Chroma level adjustment
   Adjust C ADJ so that the respective colors from B output amplitude, become 0.75Vp-p.

Operation

1. Sync separation system
   The sync separation system clamps the sync tip of the video signal having been input from pin 27 to separate the sync signal from the input video signal. Sync pulses are then processed to form BF, H, and BLK pulses, which are supplied to subsequent circuits. Of these pulses, sync and BF pulses are output at pins 2 and 3, respectively, after transformed to TTL level via buffer.

2. Luminance signal regeneration system
   Video signal input from pin 27 has its pedestal clamped, and amplified by the Y amplifier.

3. ACC system
   The burst component of the chroma signal having been input from pin 24 is detected at ACC DET. Feedback to ACC AMP occurs depending on the detected output so that the burst level is kept constant.

4. APC system
   After the signal level is brought to the fixed value at ACC AMP, the burst component alone goes into the APC circuit via the BURST GATE circuit. Meanwhile, a 0° carrier and a 90° carrier are formed from VXO output, and the 90° carrier goes into APC via the HUE circuit. At APC, phase comparison is carried out between the 90° carrier and the input burst, and feedback to VXO is performed so that the phase difference is 90° . The 0° and 90° carriers thus formed are supplied to B-Y DEM and R-Y DEM, respectively. Therefore, demodulation axis can be changed by rotating the phase of the 90° carrier at the HUE circuit.

5. Color signal regeneration system
   1) NTSC system
      The chroma signal amplified at ACC AMP is amplified again at CHROMA AMP, then demodulated at B-Y DEM and R-Y DEM, and output at pins 16 and 17 in the form of color difference signal.

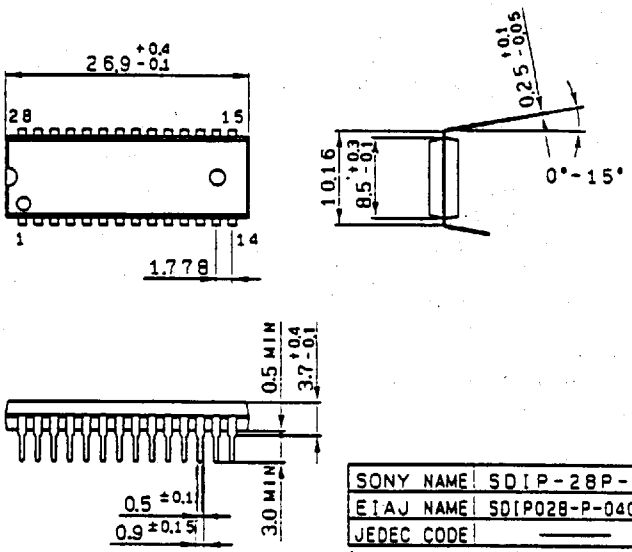
   2) PAL system
      Processing is the same as with the NTSC system up to CHROMA AMP.
      The chroma signal output at pin 21 goes into DL AMP at pin 19 via 1 H DL and DAT, and then input to the ADD/SUB circuit after level-controlled. At the ADD/SUB circuit, the signal is subjected to addition and subtraction with respect to the original signal. The signals obtained by addition and subtraction are input to B-Y DEM and R-Y DEM, and demodulated by the 0° carrier and the 90° carrier inverted every H. After that, the signal is output in the form of color difference signal as with the NTSC system.

6. PAL ID
   The PAL signal is transmitted with its R-Y component inverted every H. It is therefore necessary to inverse the demodulation axis every H. In this IC, the 90° carrier is inverted in synchronization with H BLK pulses, and checking for correspondence with the input burst is performed by synchronous detection. If an error is detected, feedback to FF (Flip Flop) is performed for correction.

T-77-29

Package Outline Unit : mm

28pin SDIP (Plastic) 400mil 1.7g



SONY NAME	SDIP-28P-01
EIAJ NAME	SDIP028-P-0400-A
JEDEC CODE	———