GRAPHICS
Enhanced Video Display Processor
V9948 E-VDP-II

PRELIMINARY

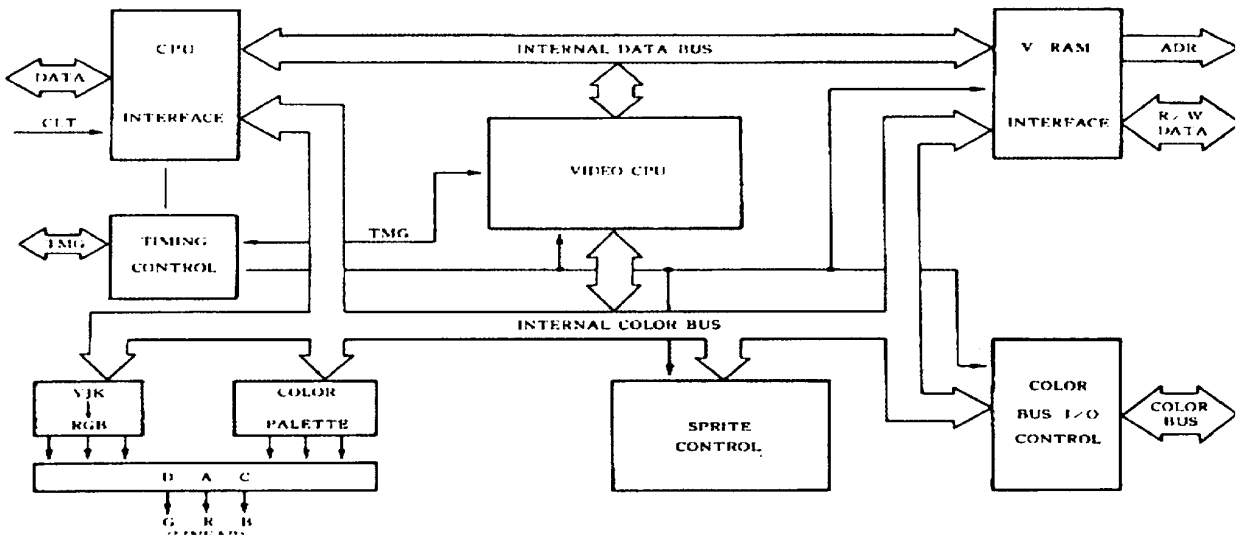
■ OUTLINE

The V9948 (E-VDP-II) is a video display processor (VDP) using an N-channel silicon gate MOS and a 64-pin shrink DIL plastic package. It is software compatible with TMS9918A and V9938.

■ FEATURES

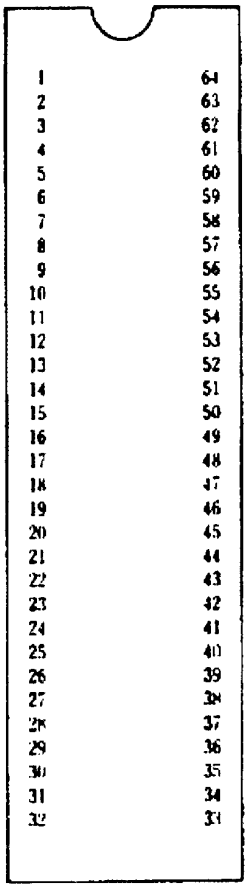
- 5V power supply.
- Outputs linear RGB.
- Built-in color palette for display in up to 512 colors.
- Capable of simultaneous display of 19.268 colors by using YJK system display.
- Capable of displaying up to 512 x 424 pixels ant 16 colors.
- Bit mapped graphics.
- Capable of displaying maximum of 256 colors simultaneously.
- 16K byte – 128K byte useable for display memory.
- Up to 128K byte expansion character video RAM/ROM can be connected.
- 16K x 1b, 16K x 4b, 64K x 1b and 64K x 4b DRAMs are useable.
- 256 addresses, 4ms auto refresh function of DRAM.
- Eight sprites can be displayed for each horizontal line.
- Colors for sprites can be specified for each horizontal line.
- Area move, line, search and other commands.
- Command function useable in every display mode.
- Logical operation function.
- Addresses can be specified by coordinates.
- Capable of external synchronization.
- Capable of superimposition.
- Capable of digitization.
- Multi E-VDP-II configurations are possible.
- External color palettes can be added by utilizing color-bus output.
- Vertical and horizontal scroll function.
- Wait function to CPU.

■ E-VDP-II BLOCK DIAGRAM



■ E-VDP-II PIN LAYOUT AND FUNCTIONS

Pin Name	Pin No.	I/O	Function
CD0 LSB	40	I/O	CPU data bus
CD1	39	I/O	"
CD2	38	I/O	"
CD3	37	I/O	"
CD4	36	I/O	"
CD5	35	I/O	"
CD6	34	I/O	"
CD7 MSB	32	I/O	"
MODE 0	29	I	CPU interface-mode select
MODE 1	28	I	"
$\overline{CSR}$	31	I	CPU-E-VDP-II read strobe
$\overline{CSW}$	30	I	CPU-E-VDP-II write strobe
RD0 LSB	41	I/O	VRAM data bus
RD1	42	I/O	"
RD2	43	I/O	"
RD3	44	I/O	"
RD4	45	I/O	"
RD5	46	I/O	"
RD6	47	I/O	"
RD7 MSB	48	I/O	"
AD0 LSB	49	O	VRAM address bus
AD1	50	O	"
AD2	51	O	"
AD3	52	O	"
AD4	53	O	"
AD5	54	O	"
AD6	55	O	"
AD7 MSB	56	O	"
$\overline{RAS}$	62	O	VRAM row address strobe
$\overline{CAS\ 0}$	61	O	VRAM column address strobe 0 (first half of VRAM)
$\overline{CAS\ 1}$	60	O	VRAM column address strobe 1 (last half of VRAM)
$\overline{CAS\ S}$	59	O	VRAM column address strobe S (for expansion VRAM)
R/$\overline{W}$	57	O	VRAM write strobe
G	22	O	Linear RGB signal output
R	23	O	"
B	24	O	"
$\overline{YS}$	10	O	Signal for switching between E-VDP-II RGB output and external video signals. (For superimpose) $\overline{YS}$ = High: E-VDP-II output is transparent $\overline{YS}$ = Low ; E-VDP-II output is not transparent
BLEO	7	O	Indicates No. 1 field/No. 2 field blanking with 3-value output. Open drain output High ; No. 2 field and active. Middle; No. 1 field and active. Low ; Linear erase interval.



Pin Name	Pin No.	I/O	Function
$\overline{\text{HSYNC}}$	5	O	High: Timig other than HSYNC or color burst timing. Low : HSYNC or timing other than color burst.
$\overline{\text{CSYNC}}$	6	O	Composite SYNC output.
CBDR	11	O	Indicates color bus direction. High: Color bus is input Low : Color bus is output
C0 LSB	19	I/O	Color bus.
C1	18	I/O	Normally color code is output. Used as input port when digitizing.
C2	17	I/O	"
C3	16	I/O	"
C4	15	I/O	"
C5	14	I/O	"
C6	13	I/O	"
C7 MSB	12	I/O	"
$\overline{\text{DHCLK}}$	2	O	Dot clock output at high resolution. Approx. 10.74MHz open drain output.
$\overline{\text{DLCLK}}$	3	I/O	Dot clock output at low resolution. Approx. 5.37MHz open drain output. As input is also possible by using the mode register, it is used for multi E-VDP-II.
XTAL 1	63	I	Used for XTAL connection. Also used for input when using an externally generated clock.
XTAL 2	64	I	
CPUCLK/ $\overline{\text{VDS}}$	8	O	1/6 of XTAL frequency is output. VRAM data select $\overline{\text{VDS}}$ = Low : VRAM access for display data. $\overline{\text{VDS}}$ = High: VRAM access for other than the above.
$\overline{\text{INT}}$	25	O	CPU interrupt output, open drain output Low: Generates interrupt.
$\overline{\text{RESET}}$	9	I	Each circuit in E-VDP-II is initial reset.
$\overline{\text{VRESET}}$	4	I	VSYNC input.
$\overline{\text{HRESET}}$	27	I	HSYNC input.
$\overline{\text{WAIT}}$	26	O	Wait signal to CPU is output.
V_{DD}	58	I	5V power supply.
GND	1	I	Ground 0V.
GND•DAC	20	I	Ground 0V.
V_{DD}•DAC	21	I	5V power supply.
V_{BB}	33	O	Baseboard voltage.

■ E-VDP-II CIRCUIT DIAGRAM